ASTRI SST-2M CAMERA RELATIVE CALIBRATION PROCEDURES

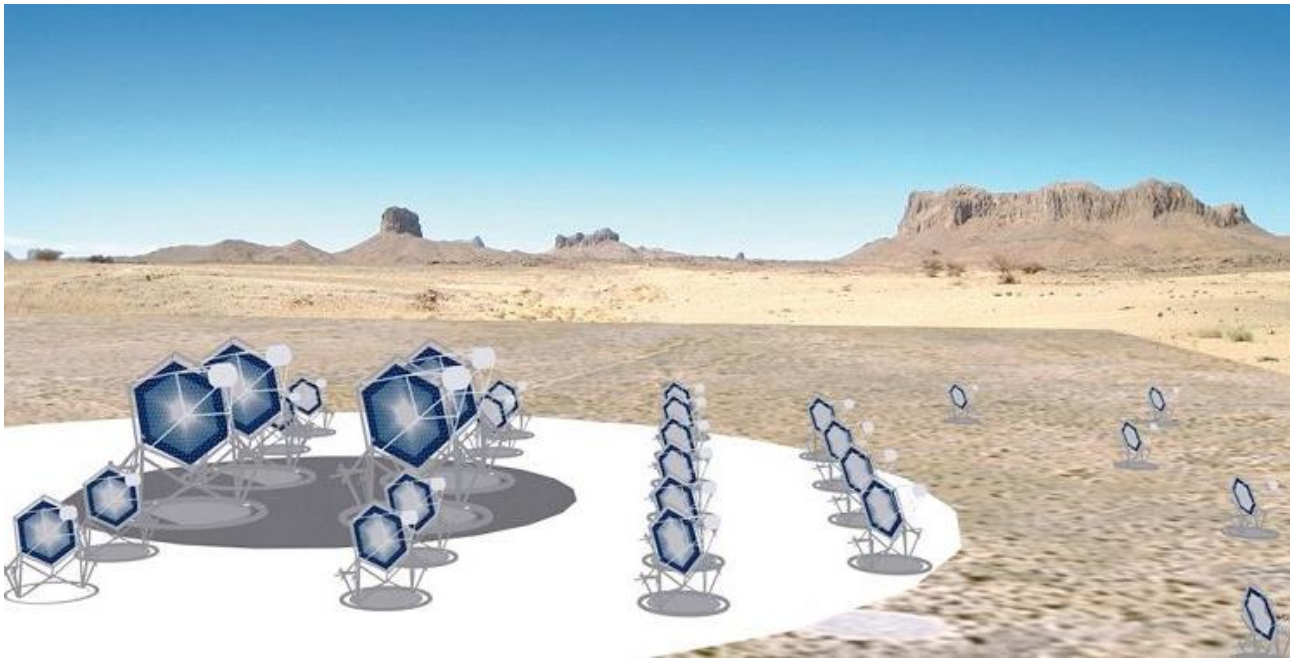

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TABLE OF CONTENTS

DISTRIBUTION LIST

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DOCUMENT HISTORY

Version	Date	Modification
1.0	29 July 2014	first version

LIST OF ACRONYMS

Vop	Operating Voltage
SiPM	Silicon Photo-Multiplier
CITIROC	Cherenkov Imaging Telescope Integrate Read Out Chip
ASIC	Application Specific Integrated Circuit
FSC	Focal Surface Camera
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
LG	Low Gain
HG	High Gain
LGS	Low Gain Shaper
HGS	High Gain Shaper
BFS	Bipolar Fast Shaper
PHD	Pulse Height Distribution
pe	photo-electron
$\mathrm{pe_{eq}}$	photo-electron equivalent
PDM	Photon Detection Module
PCB	Printed Circuit Board
CTA	Cherenkov Telescope Array
RGB-LED	Red Green Blue Light Emitting Diode

APPLICABLE DOCUMENTS

[AD1] "International vocabulary of metrology — Basic and general concepts and associated terms (VIM)", JCGM 200:2008, International Bureau of Weights and Measures

[AD2] LM-60 reference datasheet: http://www.ti.com.cn/cn/lit/ds/symlink/lm60.pdf

REFERENCE DOCUMENTS

[RD1] **ASTRI-TR-OACT-3200-007**: MPPC Hamamatsu CHARACTERIZATION REPORT

[RD2] **ASTRI-TR-OACT-3200-009** : MPPCs Electrical Characterization Report

[RD3] **ASTRI-DES-IASFPA-3200-005** : Camera Design Document

[RD4] **ASTRI-IR-IASFBO-3700-026** : ASTRI Camera Server/ ASTRI Camera Interface Control Document

[RD5] **ASTRI-TR-OACT-3200-008** :ASTRI Camera PDM: grouping four single pixels of each monolithic MPPC 4433 in four macro-pixels

[RD6] **ASTRI-DES-IASFPA-3200-008** : Geometry of the Camera Focal Surface

[RD7] **ASTRI-TR-OACT-3200-013**: Systematic Calibration Procedure for the Temperature Sensors of the SiPM Interface Boards

[RD8] **ASTRI-PLA-IASFMI-3400-001** : ASTRI verification Plan

[RD9] **ASTRI-PRO-IASFPA-3200-001** : The ASTRI SST-2M Prototype. Reference Guide to the Operational Procedures.

1. INTRODUCTION

This document describes the ASTRI SST-2M camera relative calibration procedures to be firstly performed in lab. The consolidation of lab measurements on current SiPM (Silicon Photo-Multiplier) sensor (Hamamatsu MPPC S11828-3344M) coupled with CITIROC (Cherenkov Imaging Telescope Integrate Read Out Chip) ASIC (Application Specific Integrated Circuit) read out, allows to finalize the final camera end-to-end relative calibration procedures. These guide-line procedures should be unaffected by different (better) light sensors to be used in the ASTRI/CTA mini-array cameras and represent the best compromise between complexity and required accuracy for the FSC (Focal Surface Camera). The SiPM model Hamamatsu S11828-3344M is formed by 4×4 squared physical pixels that, to match the angular resolution of the telescope optical system, are grouped 2×2 in the so-called logical (or camera) pixels, each of them corresponding to a single electronics channel. The aggregation of 8×8 camera pixels forms the so-called Photon Detection Module, PDM, related to 64 electronics channels. A matrix of PDMs forms the camera at the focal surface and, eventually, the ASTRI SST-2M camera consists of 1984 channels (or simply pixels) that individually exhibit different gains and operate at different temperatures. Table 1 summarizes SiPM trade-off specifications that should be taken into account when using SiPM underlining the characteristics that change when applied voltage (reverse Voltage) and ambient temperature are changed.

	Gain	Dark count	Crosstalk	Afterpulse	PDE	Time resolution
Increasing reverse voltage	△	△	△	△	△	△
Decreasing reverse voltage	▼	▼	▼	▼	▼	▼
Increasing ambient temperature (at constant gain)	-	△	-	▼	-	-
Decreasing ambient temperature (at constant gain)	-	▼	-	△	-	-

△: Increases
▼: Decreases
- : Depends on conditions (or does not change)

Table 1 – Influence of reserve voltage and temperature variations onto the SiPM specifications.

Although the calibration procedures described in this document are optimized for the current SiPM (Hamamatsu MPPC S11828-3344M), they are still valid for new SiPM sensors. Mitigation of critical parameters are expected for new brand of SiPM where:

- Adopting internal metal quenching resistor reduces resistance temperature coefficient of ~1/5 of the previous type lowering the requirement for the precision of the temperature measurement and voltage setting.
- Reduction of dark counts and after-pulses are obtained with higher purity of silicon.
- Optical trenches between micro-cells reduce drastically optical cross-talk allowing to operate the sensor close to the saturation where photo-detection efficiency shows a weaker dependence on temperature.
- Through-Silicon Via technology allows to tile several sensors together with almost no gap in between (better geometrical filling factor).
- Monolithic sensor (pixel) of desired size can be obtained on request.

To be coherent with the signal processing chain, all the procedures refer to the processing and read-out performed with CITIROC that is the current front-end electronics of the ASTRI SST-2M camera.

The relative calibration procedures developed and formalized in this document are the necessary starting points for performing the "on field" camera calibrations without the aid of external instrumentation.

The camera calibration does not provide the final absolute calibration of the ASTRI camera. Absolute calibration must include the transmission efficiencies of other components as mirrors and PMMA window and take into account structure obscuration, SiPM PDE and so on.

2. SCOPE

The scope of calibration, in general, is primarily devoted to "establish a relation between the quantity values with measurement uncertainties provided by measurement standards and corresponding indications with associated measurement uncertainties (of the calibrated instrument) and, in a second step, uses this information to establish a relation for obtaining a measurement result from an indication" [AD1].

Calibration is of paramount importance to fully describe the response function of the camera. In particular, trigger stability and energy resolution at a few percent of accuracy are required.

The diagram in Figure 1 illustrates the correlations and parameter ranges between the major physical quantities that need to be taken into account for implementing successfully the calibration procedures.

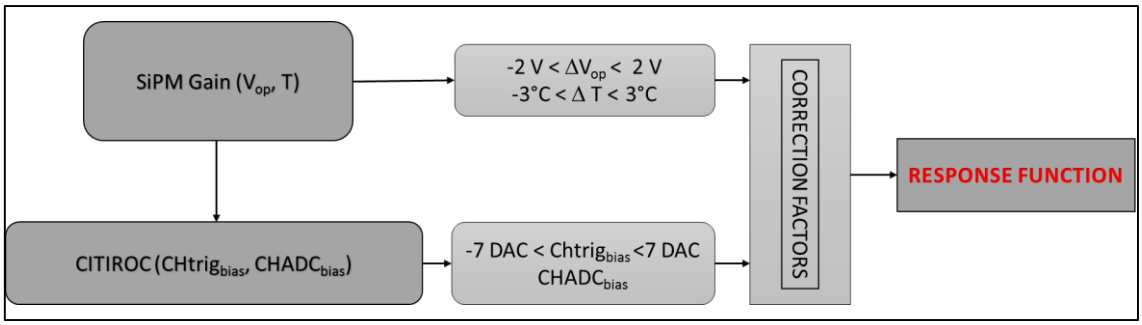


Figure 1: Physical quantities involved in the calibration procedures.

The SiPM gain depends from the operating voltage as well as from the temperature according to the following equations:

$$G(V,T) = \frac{dG}{dV} \cdot V_{op}(T_0) \qquad (1)$$

$$G(V,T) = \frac{dG}{dT} \cdot T + G(V_0, T_0) \qquad (2)$$

where $\frac{dG}{dV}$ is the gain variation coefficient as a function of the voltage, $V_{op}(T_0)$ is the SiPM operating voltage at a given temperature, $\frac{dG}{dT}$ is the gain variation coefficient as a function of temperature and $G(V_0, T_0)$ is the gain at a given operating voltage and temperature.

Combining linearly (1) and (2) and posing $\frac{dG}{dV} = c_1$, $\frac{dG}{dT} = c_2$ *and* $G(V_0, T_0) = c_3$ the resulting equation is:

$$G(V,T) = c_1 \cdot V_{op} + c_2 \cdot T + c_3 \qquad (3)$$

Gains equalization are determined by minimizing the weighted mean square error between the measured data y_i and the best fit function $G(V_i,T_i,a,b,c)$, where *n* is the number of measured data points:

$$\sum_{i=0}^{n}(y_i - G(V_i, T_i\ , c_1, c_2, c_3))^2 \qquad (4)$$

Equation (4) with an opportune change of variables, strictly connected with the available measurable quantities (ADC counts, DAC codes and temperatures), represents the leading algorithm for gain equalization.

In Figure 1 channels ADC bias has operative interval not specified because it depends on the bias (pedestal) that CITIROC introduces, slightly different channel by channel. This cannot be corrected a priori and need to be recorded in a "pedestals data base". Although the values of the pedestals do not change as the temperature changes is still convenient to record their values at the beginning and end of each scientific run.

First level trigger signal equalization is the other topic of fundamental importance for carrying out an effective and robust relative calibration of the camera. As the first level trigger signals are at the base of the acquisition of the physical event, trigger equalization and hence stability are essential for a correct and reliable camera operation. As for any multi-channel electronics Front-End, small differences between trigger channels are expected. The causes of such non-uniformity are numerous although usually small differences in voltage reference of the discriminators are the main issue. CITIROC allows to correct, for some extent, this kind of non-uniformity between channels. Triggers equalization will be performed once that the channels equalization has been performed.

SiPM pixel dark noise rate is about 1 MHz at 25 °C. Dark noise rate is not considered in the calibration parameters being negligible compared to about 21 MHz of a Moon-less NSB (Night Sky Background). Its variation with temperature produces a slight variation of the dispersion around mean photo-electrons value. This effect, however, will be quantified too.

3. SIGNAL PROCESSING AND DEFINITIONS

A schematic view of the typical signal processing path of CITIROC channels is given in Figure 2. This oversimplified scheme actually involves the whole signal processing chain and is valid for each channel (pixel) of the camera. This description is intentionally very brief. More details on SiPM characterization and CITIROC front-end electronics are given in [RD1,RD2] and [RD3] respectively.

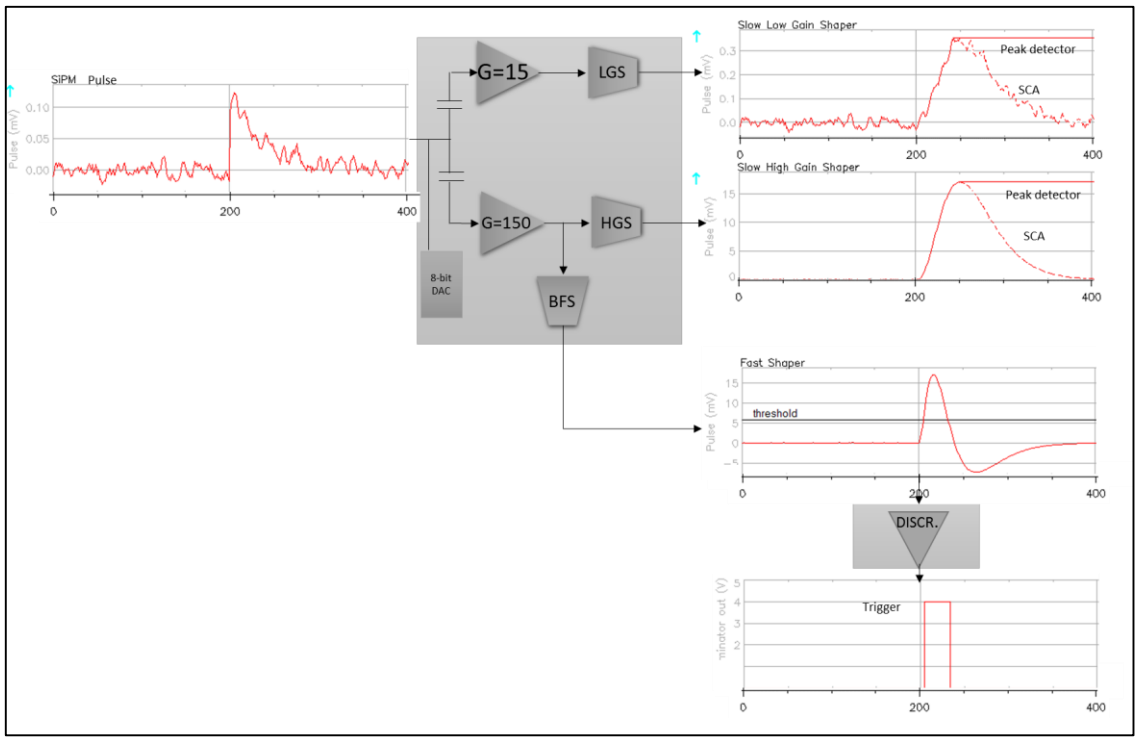


Figure 2: Signal processing path of one CITIROC channel.

Each CITIROC channel implements an 8-bit DAC for SiPM gain adjustment. The pulse generated by SiPM is processed by the AC coupled CITIROC electronic channel. It is amplified by means of two programmable preamplifiers (nominal Gain=15 for LG and nominal Gain=150 for HG) and then shaped (nominal shaping time = 37.5 ns) with two shaper circuits (LGS and HGS) respectively. A bipolar fast shaper (BFS) connected to the high gain preamplifier (nominal Gain=150) produces a fast signal (~15 ns shaping time) that is connected to a discriminator with 10 bits-DAC programmable threshold. The output of the discriminator gives a digital signal (trigger) if the signal exceeds the threshold level. The top-right plots, showing the low gain shaper and high gain shaper, represent the two modes of operation of the ASIC: peak detector (continuous line) or single channel analyser (dash line). The base-line operational mode is peak detector. The maximum of the shapers represents the pulse height conversion of the SiPM input signal. The digital triggers (64 channels for each PDM) are available on the 32 + 32 output pads of the two ASICs constituting the unit PDM module based on 64 pixels. The analog outputs of the peak detectors are stored into 64 analog memories and read, at

the occurrence of a trigger condition, by multiplexing the three-state output registers (LG and HG respectively) and then converted to digital counts by external ADC devices. An Artix 7 FPGA governs and controls all the input/output operations from/to CITIROCs and SiPMs.

Taking into account the signal processing operational mode above mentioned, it is convenient to describe the measurements needed for the implementation of the relative calibrations method. Let us define:

- **Pulse Height Distribution (PHD)** as the variation of the height of the output pulses at a given applied voltage and discriminator threshold sampled in a given time. This variation is caused and changes proportionally to the light intensity seen by the SiPM and/or by self-produced dark current pulses.
  PHD is generally used to measure the distribution of intrinsic dark current of the sensor and to measure the sensor response to pulsed or continuous light.

- **Rate Curve (Stair)** as the variation of the number of output pulses at a given applied voltage and discriminator threshold sampled in a given time. This variation is proportional to the light intensity seen by the SiPM.
  Stair, so called for its characteristic shape, is generally used to measure the intrinsic dark current rate (self-produced pulses) and to measure the sensor response to pulsed or continuous light in terms of number of triggered pulses in a given time. Stair measurement gives also an estimation of optical cross-talk.

Pulse Height Distributions and Stairs are at the base of the calibration procedures and they are referred as Dark PEQ (photo-electron equivalent), Fiber PEQ, Dark Stair and Fiber Stair in the “ASTRI Camera Server / ASTRI Camera Interface Control Document” [RD4].

4. SIGNAL CONDITIONING CAPABILITIES

Signal conditioning capabilities refer to the ability to manipulate the analog signals in such a way that they meet the requirements of the next stage for further processing. In our case several conditions concur to this process as for example SiPM temperature dependence, front-end gain sensibility and linearity, housekeeping signals that must be normalized and filtered to levels suitable for analog-to-digital conversion and so on.

The end-to-end signal conditioning includes all of these effects. This implies the need to characterize all the 1984 electronics channels starting from the analog SiPM signals to the converted digital signals. In this way is possible to obtain a camera-electronics relative calibration transfer function that is closely related to the complete electronics signal path. Temperature ranges matching, operative voltages setting and signal to noise optimization are the main parameters that need to be tuned. The relative calibration is just the tool to perform and test the accuracy of signals conditioning.

4.1 Geometry and SiPM placement on PDM and on FSC

According to the results reported in [RD6] and related to all the 528 MPPCs currently available, the histograms of the mean value of the operating voltage, V_{op}, and the deviation from the V_{op} with respect to its mean value for each logical pixel are shown in Figure 3. The V_{op} is defined as the SiPM operating voltage at temperature of 25 °C and resulting gain of 7.5 x10^5. Recalling that a logical pixel consists of 4 physical pixels tied together, a mean value of V_{op} and a deviation from the mean V_{op} is expected. Grouping four independent physical pixels produces also a lower signal amplitude (~1/4) with respect to one physical pixel. While the logical pixel selection criteria adopted for populating the focal surface is described in [RD5] following the geometrical convention given in [RD6], here the outcome of this survey is used to infer the boundary conditions for implementing the gain equalization procedures.

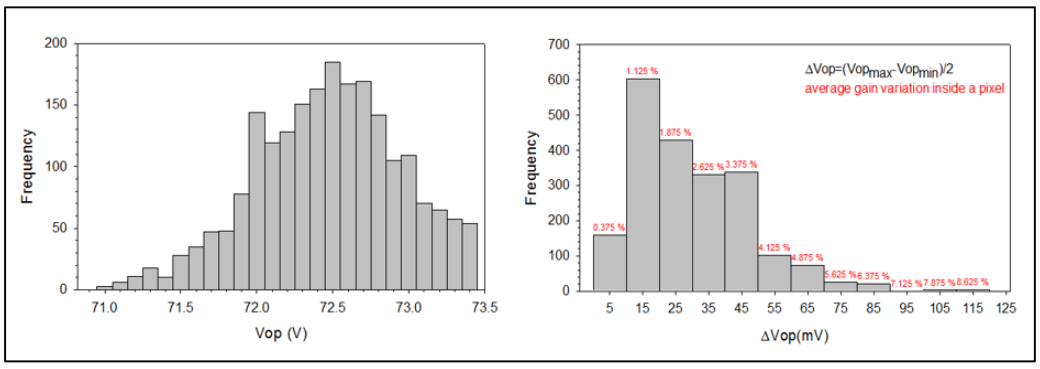


Figure 3: The histogramed V_{op} of all the logical pixels (left).The histogrammed ΔV_{op} (right). In red the expected averaged gain variation of the binned logical pixel as a function of ΔV_{op}.

From the above histograms results that all pixels operating voltages are in the range of 71 V < V_{op} < 73.5 V (at 25°C and gain of 7.5 x10^5) while in order to have an average gain dispersion less than ~ 4%, within a logical pixel, ΔV_{op} must be

less than 65 mV. Almost the entire focal surface, 1965 logical pixels out of 1984 exhibit these values while in the central part of the FSC (25 PDMs) the inter-pixels gain dispersion is below 2.5%.

PDM mean V_{op} values are also reported in Figure 4. These values are defined as the arithmetic mean of the minimum value and the maximum value of V_{op} of each PDM. Figure 4 shows the minimum, maximum and mean V_{op} values for the 25 PDMs located in the central part of the FSC.

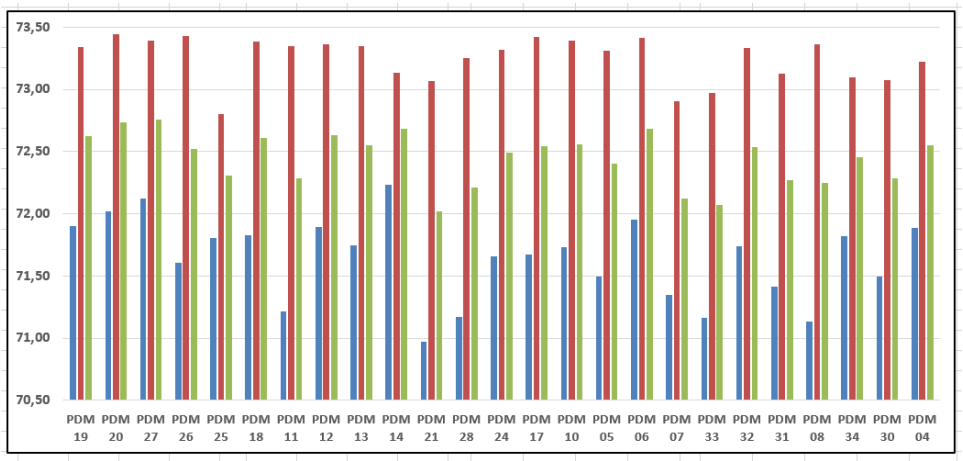


Figure 4: Distribution of minima (blue lines), maxima (red lines) and mean V_{op} (green lines) values of the 25 PDMs, ordered according to their inter-pixel gain dispersion (see Figure 6).

According to the geometrical convention given in [RD6], the PDMs and pixels numbering inside each PDM are as those shown in Figure 5.

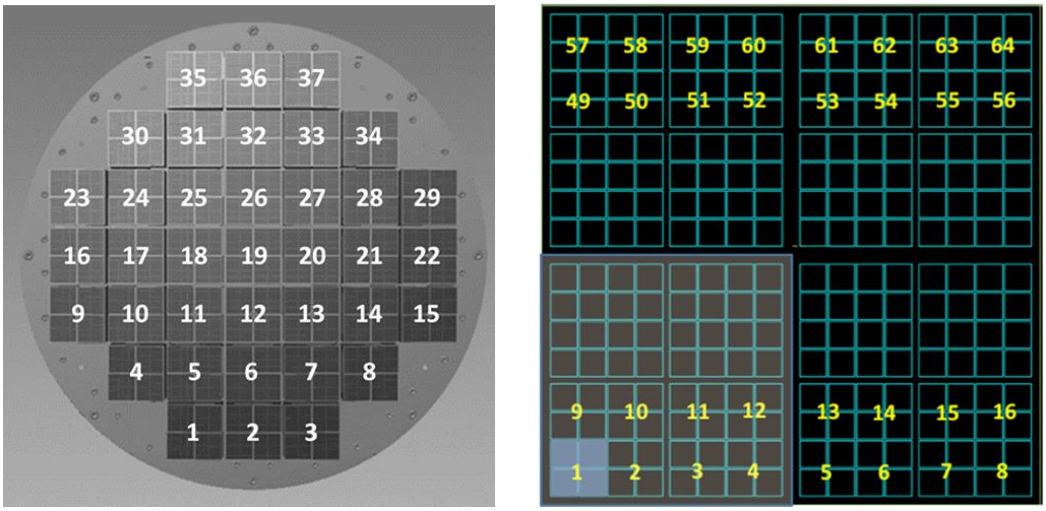


Figure 5: Numbering of the 37 PDMs forming the focal surface and the PDM pixels.

The placement of PDMs on the FSC follows the adopted geometrical convention. PDM PCBs (Printed Circuit Board) are populated with SiPM monolithic chips

which have the closest V_{op} within a logical pixel (formed by 4 physical pixels). Starting from the center of FSC (PDM n. 19) and going towards the FSC periphery, PDMs are symmetrical placed on FSC with gradually degrading inter-pixels gain dispersion.

While this configuration optimizes and keeps almost uniform (actually gain dispersion values gradually increase towards the FSC periphery) camera pixels at level of inter-pixels gain dispersion, so it is not for the operating voltage of pixels. Each V_{op} logical pixel can have any value between 71 V and 73.5 V and then it needs to be adjusted to its actual operating voltage. Figure 6 shows the arrangement of PDMs on the FSC ordered by ordinal numbers (in red) representing PDMs increasing inter-pixels gain dispersion as given by the histogram on the right of Figure 3.

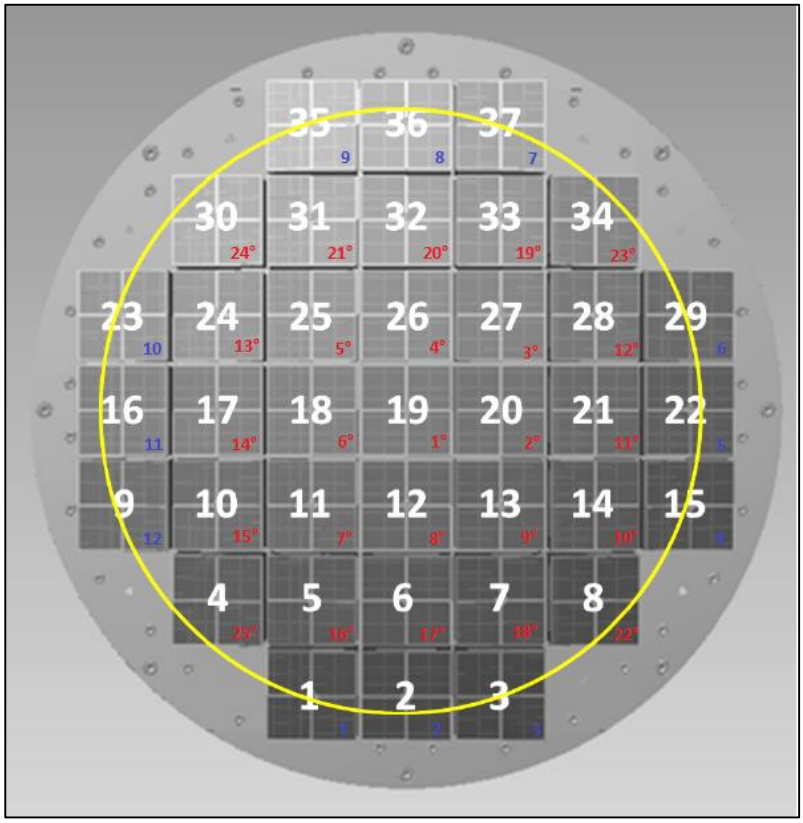


Figure 6 : PDMs arrangement as a function of the inter-pixel gain dispersion (red number).

The histogram of the V_{op} should be corrected for the desired reference operating temperature and gain. This will be done once that the dG/dV and dG/dT coefficients, representing respectively the gain variation as function of applied V_{op} and temperature, will be deduced from the measurements (see in Annex A how change the V_{op} after the corrections for gain and temperature).

4.2 Lab. Experimental Set-Up

To define the calibration procedures for the camera, some preliminary work is needed on the whole channel chain (SiPM + CITIROC + ADC + FPGA) in order to establish the relations between the several parameters that concur to the desired performance. This work has been carried out using the available instrumentation in the laboratories of OACT-Catania and IASF-Palermo. The current report is focalized on the measurements performed using the set-up shown in Figure 7; a picture of the light-tight box is shown at the bottom.

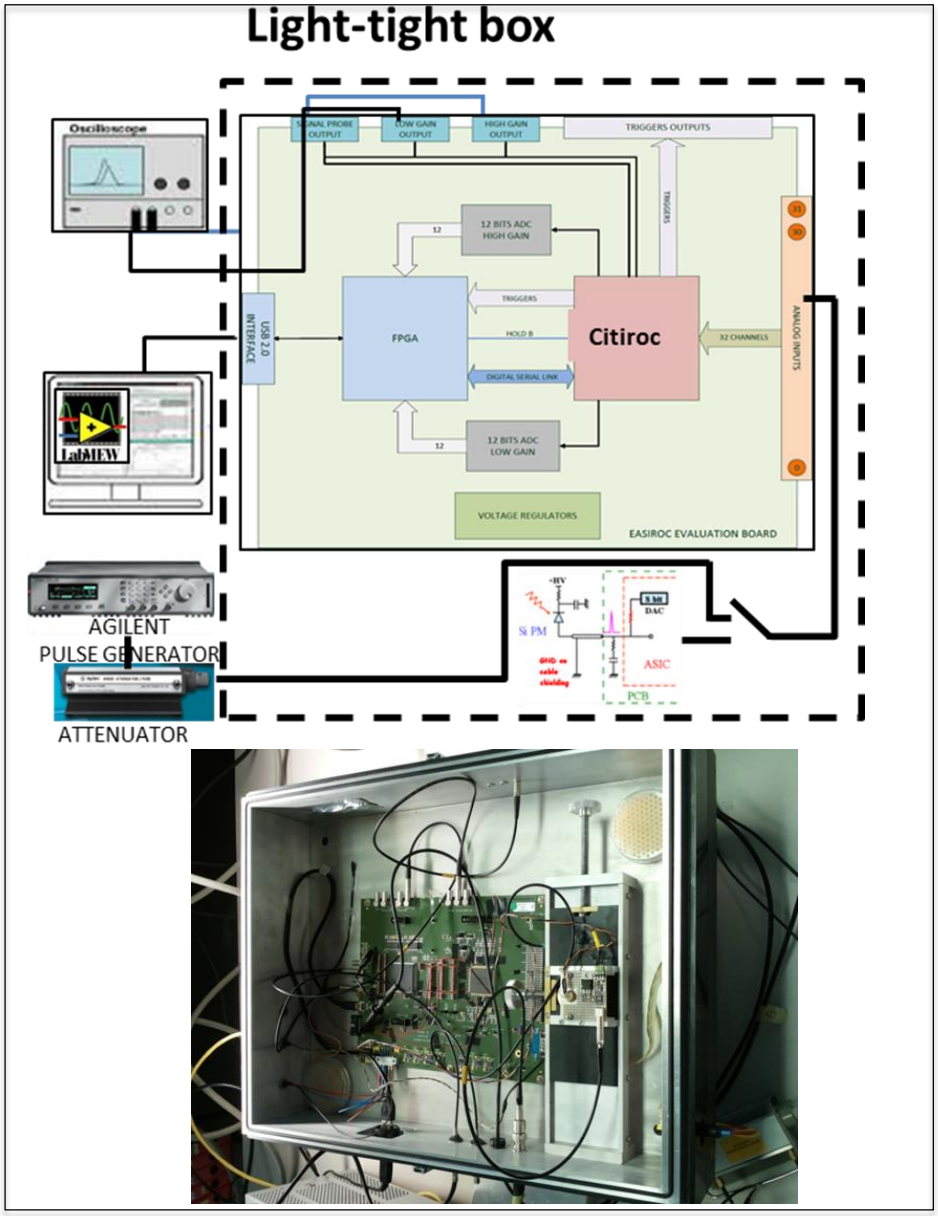


Figure 7: Experimental set-up. A light-tight box coupled with a Peltier Cooling/Heating system assures a constant temperature on the SiPM under test with stability of ~ 0.1°C.

The Lab. instrumentation used for the measurements is the following:

1) Oscilloscope Lecroy LC 684D 1.5 GHz
2) Signal generator Agilent 81160A
3) 2 Attenuators Agilent 8494A ed 8495A
4) High impedance Tester Keithley 2000
5) PC - Windows 7
6) Programmable Voltage Generator Agilent N6705B
7) CITIROC evaluation board
8) SiPM 4x4 pixel chip Hamamatsu S11828-3344M
9) Thermal controlled Box with light generator fiber

while the software tools used, including Microsoft Office 2010, are:

a) Agilent 33503A Benchlink Waveform Builder Pro Software
b) Simulated SiPM pulses (IDL custom code)
c) EASIROC Evaluation board LABVIEW software

The set-up for the temperature sensors calibration consists of a system manufactured by LakeShore and a calibrated temperature diode as shown in Figure 8.

Figure 8: LakeShore temperature measurement system. On the blue box is visible the calibrated temperature sensor.

The set-up shown in Figure 7 is used only for verification purposes. Functional parameters and relations between them are carried out using only SiPM and CITIROC front-end. Light pulses, when needed, are generated by pulse generator coupled to a RGB-LED facing the SiPM pixels.

The light pulses in the camera will be generated by the same RGB-LED driven by a fast pulse generator located inside the camera that, illuminating its PMMA transparent protective window, provides similar luminous signal-pulses.

4.3 Channels Tuning and Parameters Extraction

The expected average and gradient temperature inside the camera as well as the differences in V_{op} between pixels and the desired minimization of pixel optical cross-talk leads to define a reference SiPM operating voltage and a reference temperature. A method for SiPM cross-talk evaluation is described in Annex B. To ultimately define the relative calibration procedures, a series of measurements on specific aspects involving the signals processing have been carried out in laboratory making use of the set-up above mentioned. As seen in Section 3, PHD and Stair measurements are the base of the relative calibration procedures. This means that the measurable quantities are: DAC-input gain-adjustment, threshold discriminator DAC, ADC counts and pixels temperatures. In the following discussion physical quantities are converted to these units.

4.3.1 HG and LG dynamic range and linearity

Dynamic range refers to the range of values that can be measured by a sensor and associated front-end. The dynamic range of measurement is limited at one extreme by saturation of the combined response of signal sensor and proximity electronics. The other extreme of the dynamic range of measurement is often limited by one or more sources of random noise or uncertainty in signal levels that may be described as the sensitivity of sensor and electronics.

In our case, to fulfil the CTA requirements, the dynamic range must extend from 1 photo-electron to 1000 photo-electrons. Achieve three order of magnitude in dynamic range is not trivial. CITIROC provides such a dynamic range using two chains: High Gain and Low Gain chains integrated in the ASIC. Amplification gain for each chain is programmable from 10 to 150 and from 1 to 15 (nominal values) for HG and LG respectively. Establish the working dynamic range of a system is usually a compromise between signal resolution and required working range. As the useful range increases the resolution decreases and vice versa. Moreover the check of the response linearity is mandatory in order to extract the needed parameters and correction factors useful for simulations and data analysis.

The HG and LG dynamic ranges and related linearity response are shown in Figure 9. This set of measurements have been carried out using Agilent pulse generator and attenuators. Simulated SiPM-like signals corresponding to a gain of 7.5×10^5 and from 1 to more than 1000 equivalent pe are sent to channel 22 of the evaluation board. Mean value and standard deviation of pulse height distribution (CITIROC operates in peak detection mode and shaping time set to 37.5 ns) are computed, for increasing in charge signals, by the LAB VIEW interface program, stored in the PC disk and then plotted.

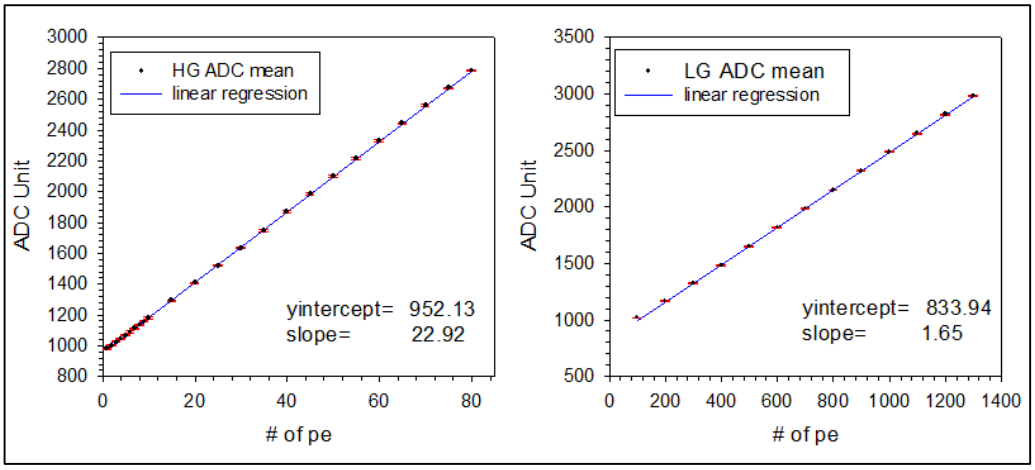


Figure 9: HG and LG pulse height distribution linearity for nominal amplification gain of 150 (HG) and 15 (LG) respectively.

The HG dynamic range extends from 1 to 80 pe, with a resulting slope, as given by fitting linearly the sampled pulses height data, of 22.92 ADC/pe. This value is the reference value for calculating SiPM gain when it is expressed in ADC units. The LG dynamic range extends from 80 to 1300 pe, with a resulting slope, as given by fitting linearly the sampled pulses height data, of 1.65 ADC/pe. Note that the expected ratio between nominal amplification gains (150/15) is actually 22.92 /1.65.

4.3.2 Unknown gain determination

As stated in the previous paragraph, a reference gain value has been used to perform linearity measurement of the CITIROC analog chain. The gain, or amplification factor, is the extent to which an analog amplifier boosts the strength of a signal. The input analog signal is voltage-amplified by CITIROC. PHD allows to estimate the overall gain by measuring the mean value, in ADC units, of the distances between the peaks of the histogram produced by the input light pulses (pe). A known charge can be injected to the channel by means of a pulse (using pulse generator) that has the same characteristic of the SiPM pulse, i.e., same recovery time, same pulse height voltage and same charge. The unitary pulse (1 pe) so generated looks like an actual pulse of a SiPM pixel operating at a calculated gain of 7.5×10^5. Figure 10 shows the PHD of pulses corresponding to 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 pe.

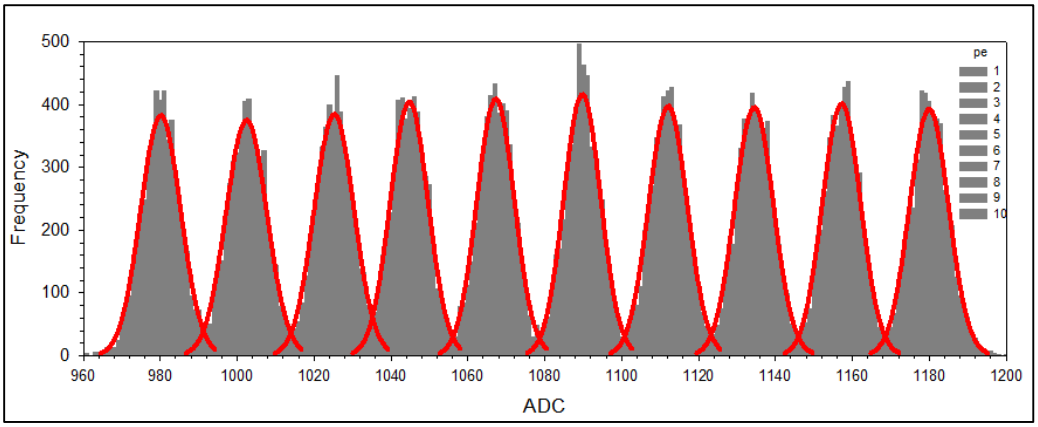


Figure 10: Histogram and Gaussian fits of generated pulses corresponding to 1,2,3,4,5,6,7,8,9,10 pe.

The mean of the distances between peaks gives the gain in ADC units corresponding to signals that look like SiPM pulses with $G(V_{op},T) = 7.5 \times 10^5$. This reference gain can be used to evaluate an unknown pixel gain using the following relations and assuming a linear dependence between gains:

$$G_1 = G_{known} \cdot G_{CITIROC} \qquad (5)$$

$$G_2 = G_{SiPM} \cdot G_{CITIROC} \qquad (6)$$

The above relations can be written as:

$$\frac{G_2}{G_1} = \frac{G_{SiPM}}{G_{known}} \qquad (7)$$

where $G_{CITIROC}$ is the electronics gain, G_{SiPM} is the unknown SiPM gain and G_{known} is the reference gain. From (7), expressing G_2 and G_1 in ADC units, straightforward calculation gives the unknown SiPM gain:

$$G_{SiPM} = \frac{G_{2ADC}}{G_{1ADC}} \cdot G_{known} \qquad (8)$$

This useful relation correlates PHD measurements with SiPM gains.

4.3.3 SiPM PCB temperature sensors calibration

The temperature sensors in each SiPM board belong to the LM-60 series by Texas Instruments [AD2]. They are precision integrated-circuit sensors allowing temperature sensing from -40°C to +125°C while operating from a single +2.7 V power supply. The LM-60 is calibrated to provide accuracies of ±2.0°C at room temperature and ±3°C over the full −25°C to +125°C temperature range.

The temperature sensors calibration of the PDM modules is an essential prerequisite for the SiPM gain equalization. In fact, temperature sensors, managed by the front-end FPGA, allow the monitoring of the SiPM pixels temperature so that input DACs of the CITIROC front-end ASICs can be set accordingly. This operation is performed in the BE for all the PDMs.

Each SiPM PCB has in total 9 temperature sensors symmetrically spaced on the rear side of the board. Only the central sensor at the bottom of the board has been calibrated using a calibrated reference diode temperature sensor, manufactured by LakeShore and biased by an appropriate temperature controller developed by the company itself. Calibration of the other eight sensors in the bottom side of the board will be easily accomplished with respect to the calibrated one at the time of the PDM test. The test procedure for temperature sensors calibration is reported in Annex A.

An exhaustive report on the calibration procedure of the temperature sensors can be found in [RD7]. Here we summarize the temperature sensors calibration results and give the formalization of the method to use for temperature sensors managing.

The nine rear side SiPM board temperature sensors are read by the FE FPGA. The multiplexed outputs are connected to a 12-bits ADC with internal reference voltage of 1.25 V, embedded in the ARTIX 7. Each PDM FE FPGA reads the related temperature sensors at a rate of about 10 Hz. This operation is not critical as we expect slow time variation of temperatures inside the camera. The read values are updated at this rate and saved in FPGA registers making them available to the BE. In the BE the temperatures for each PDM are read periodically and a software algorithm resident in one of the CPU of the BE FPGA will manage the correction, pixel by pixel, of the DAC-input according to the registered variation of temperature.

Figure 11 shows the sampled voltage values of each of the 37 PDM central temperature sensors as function of the reference calibrated temperature and the related linear fits. As is evident from the plot, the accuracy of the temperature sensors is within the one declared by the manufacturer. In fact, the maximum voltage differences at a given temperature is about 18 mV that divided by the average slope of 6 m V/°C gives approximately a dispersion around the mean value of ± 1.5 °C in the temperature range of 12 ÷ 18 °C.

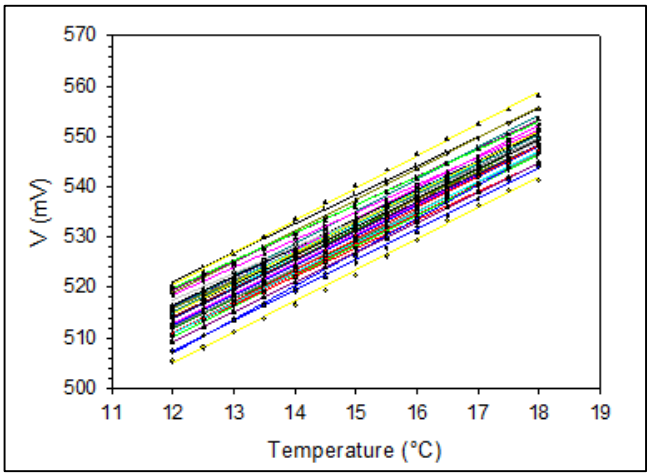


Figure 11: Sampled Voltage values of the 37 SiPM board central temperature sensors as function of temperature referred to the calibrated diode temperature sensor.

Table 2 shows the coefficients of the linear fit of each central temperature sensor of each SiPM board. Calculating the residuals for each fitted temperature sensors and dividing them for the respective **m** coefficient gives in unit of °C the maximum errors using fitted lines. This can be evaluated easily with the histogram of the dispersion of all the residuals normalized to the respective **m** as shown in Figure 12. From the histogram the line fitting introduces a maximum dispersion around the mean value of about 0.2 °C. This value must be compared with the minimum DAC-input temperature resolution which is, as shown in Section 4.3.6, about 0.25 °C/DAC, so that the coefficients of the linear fitting can be used to calculate the temperature sensor voltages.

Obviously the temperature sensor voltages must be converted in ADC values. The conversion factor of the ADC is given by $CF_{ADC}=V_{ref}/(2^{12} - 1)$ with V_{ref} in mV. The transfer function in ADC unit results:

$$V_{ADC} = \left(\frac{m * T + q}{CF_{ADC}}\right)$$

Temperature can be found resolving for T the above equation.

Table 1

PDM	m (mV/°C)	q (mV)
1	6.0754	434.2969
2	5.4621	452.9225
3	5.9793	439.2330
4	5.8388	441.6712
5	5.2473	454.4266
6	5.9796	443.3843
7	5.8993	442.0760
8	6.0215	437.8954
9	6.0313	442.5187
10	6.6921	426.5133
11	6.1780	430.6574
12	5.7100	445.4323
13	5.6608	442.8462
14	5.7258	447.6880
15	5.7030	446.5409
16	6.2481	435.9357
17	5.5897	448.8796
18	5.6460	451.7101
19	6.3725	439.4344
20	5.7952	446.6771
21	6.1720	444.6603
22	5.7688	442.8266
23	5.5480	453.0881
24	5.8820	443.3557
25	5.9222	438.1047
26	5.7410	443.1559
27	6.1877	439.7285
28	5.7242	452.4527
29	5.8852	444.4095
30	5.6711	446.2820
31	6.4187	443.3982
32	5.9313	441.2095
33	6.2401	440.0453
34	5.8755	440.5314
35	5.4125	450.9013
36	5.7409	445.0791
37	5.8964	438.5136

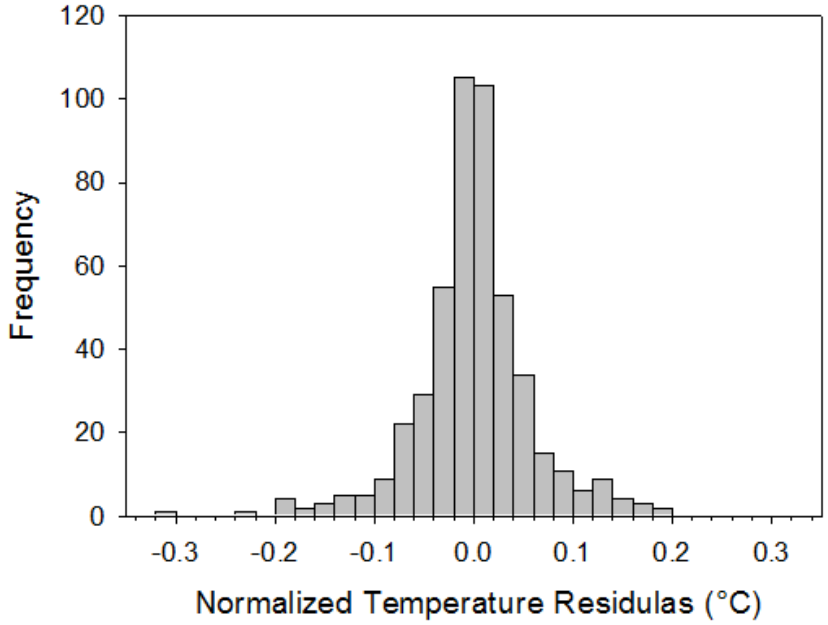


Figure 12: Histogram of the normalized temperature residuals.

4.3.4 CITIROC DAC-Input

The CITIROC front-end allows through an input programmable DAC (one per channel) to adjust SiPM pixel gain tuning its operative voltage V_{op} according to the relation:

$$V_{op} = V_i - V_{DAC} \qquad (9)$$

where V_i is the voltage at the input channel and V_{DAC} is the converted voltage corresponding to a given DAC-input code.

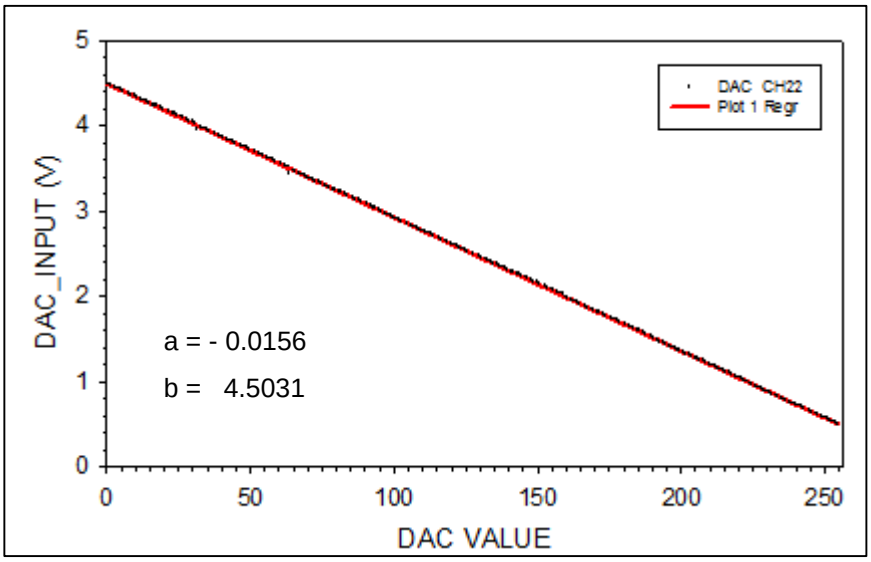


Figure 13: CITIROC evaluation board channel 22 DAC-input voltage as a function of the DAC code.

Figure 13 shows the channel 22 DAC-input generated voltage as function of DAC codes. The fitted values gives for this channel the linear equation:

$$V_{DAC} = a \cdot DAC\ (V) + b\ (V) \qquad (10)$$

The desired V_{op} can be obtained substituting V_{DAC}, as calculated in (10), into equation (9). The measurement of the DAC-input linearity is performed reading the output voltage of the DAC-input with the Keithley high impedance tester varying progressively the DAC codes. Figure 14 shows the DACs input linearity as measured in the CITIROC evaluation board. Each DAC-input channel has slightly different slope, so it is necessary to perform this measurement for each CITIROC channel. The coefficients of all the fitted line will be kept for the correction of the corresponding channel. This is a key function for the equalization of SiPMs gain that, as stated in Section 4.1, exhibit different V_{op}. In addition, local variations of the temperature (gradient) require correction of the values of the input voltage to the DACs in order to maintain constant the gain of the SiPM with respect to the reference operating temperature.

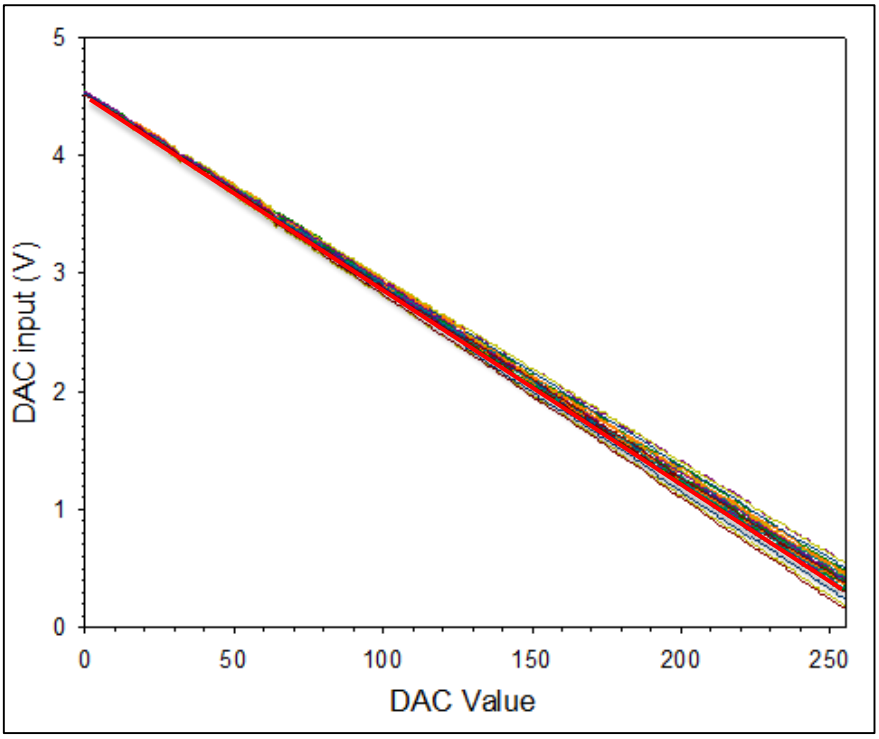


Figure 14: Measured DACs input linearity of each of the 29 CITIROC channels as measured in the evaluation board. Three channels are missing.

As can be deduced from Figure 14, V_i can be linearly adjusted channel by channel in the range 0 V ÷ 4.5 V. Taking into account the spread and the distribution of the measured SiPM V_{op} (see Figure 3), it is convenient to set V_i with V_{DAC} set in the middle of the DAC-input dynamic range, close to 128 DAC code for example, so that operating voltages can be adjusted varying the V_{DAC} of each channel with respect to this reference point. Rearranging equation (10), V_i can be expressed as:

$$V_{i0} = V_{op0} + V_{DAC0} \qquad (11)$$

where V_{op0} is the V_{op} value corresponding to the maximum frequency of the measured V_{op} of the SiPM distribution and V_{DAC0} is the voltage corresponding to the DAC-input value of 128 (or close to it) of the fitted values of the averaged DAC-input channels (red line in Figure 11) with slope a_0 and intercept b_0. Each pixel is so set to the desired gain (at a given constant temperature and constant V_0) and further adjustment of gain by means of DAC-input is only requested to correct pixels gains due to temperature variations.

Equation (10) can be used conveniently for setting V_{DAC} knowing the $\frac{dG}{dV}$ (gain variation coefficient as a function of the V_{op}) at a given constant temperature.

Once $\frac{dG}{dV}$ is deduced, the $\frac{dG}{dT}$ at a fixed V_{op} (gain) determines the gain adjustment, setting V_{DAC}, needed to compensate temperature variations.

The general relation to set V_{DAC} codes according to V_i and V_{op} may be written:

$$\begin{cases} V_{i0} = V_{op0} + V_{DAC0} \\ V_{ik} = V_{op_k} + V_{DAC_k} \end{cases} \qquad (12)$$

where V_{ik} are the applied voltages to the DAC-input channels, V_{opk} are the corresponding V_{op} of SiPM pixels and V_{DACk} are the voltages of the corresponding DAC-input values.

Solving (12) for V_{DACk} gives:

$$V_{DAC_k} = (V_{ik} - V_{i0}) + (V_{op0} - V_{op_k}) + V_{DAC0} \qquad (13)$$

Using equation (10), the (13) may be written:

$$a_k \cdot DAC_k + b_k = (V_{ik} - V_{i0}) + (V_{op0} - V_{op_k}) + a_0 \cdot DAC_0 + b_0 \qquad (14)$$

finally, solving for DAC_k, the DAC-input value corresponding to each k-th (k= 1,…..,64 PDM pixels) channel can be calculated:

$$DAC_k = \frac{(V_{ik} - V_{i0}) + (V_{op0} - V_{op_k}) + a_0 \cdot DAC_0 + b_0 - b_k}{a_k} \qquad (15)$$

DAC_0 represents the reference DAC code value (0,…., 255).

In our case, since all the 37 PDMs are powered at the same voltage, it follows that $V_{ik} = V_{i0}$ and then the equation (15) reduces to:

$$DAC_k = \frac{(V_{op0} - V_{op_k}) + a_0 \cdot DAC_0 + (b_0 - b_k)}{a_k} \qquad (16)$$

4.3.5 dG_{ADC}/dV Determination

The $\frac{dG_{ADC}}{dV_i}$ is determined using PHDs as produced by pulsing a blue LED at a constant rate of 10 kHz and time-on duration of 11.5 ns. The temperature is kept at 15 °C ± 0.1 °C and the V_i is increased with step of 100 mV from 74.11 V to 74.51 V. The DAC-input is set to 126. One of the four available logical pixel is connected to channel 22 of the CITIROC evaluation board. The resulting PHDs are shown in Figure 15.

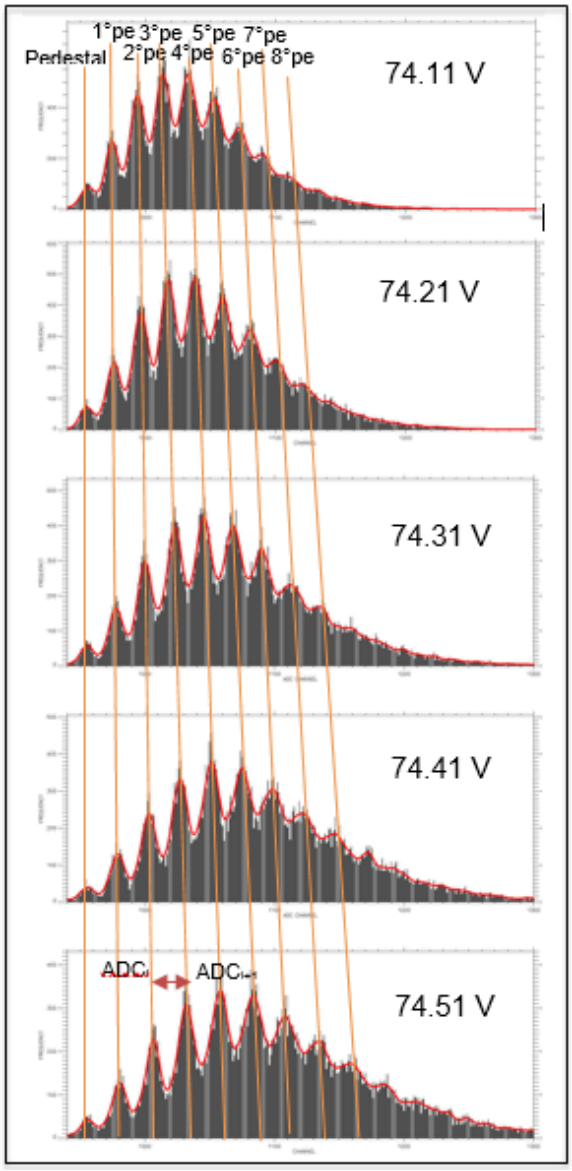


Figure 15: CITIROC Channel 22 PHDs at a fixed temperature of 15 °C as a function of the V_i. The decreasing slopes of the orange lines show qualitatively the increasing gain (distance between peaks), measured in ADC unit, as the SiPM voltage increases.

The gain of each SiPM pixel is calculated from each histogram of data gathered from the pixel and smoothed with a boxcar averaging of specified width. Gain has been obtained by determining the arithmetic mean of the distances between subsequent local maxima applying equation (16). It represents the pe equivalent gain in ADC unit. ADC_i is the ADC value of the local maximum of the i-th peak on the histograms while N is the number of peaks.

$$pe_{eq}(ADC) = \frac{1}{N} \cdot \sum_{i=1}^{N} (ADC_{i+1} - ADC_i) \qquad (17)$$

A plot of the mean distances between subsequent local maxima and associated standard deviation errors for each of the histograms of Figure 15 is shown in Figure 16.

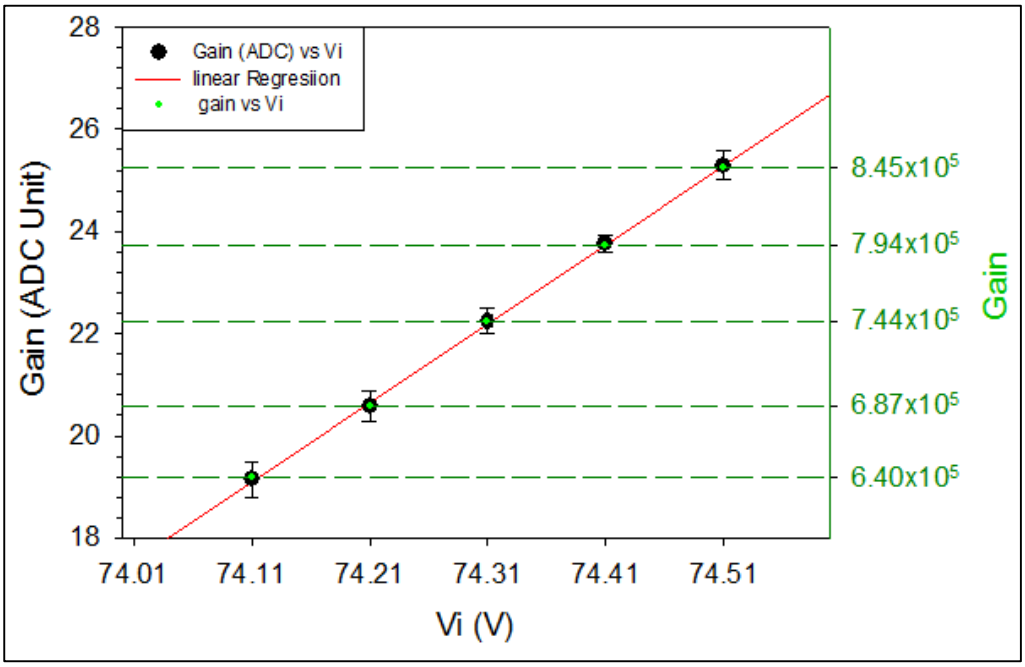


Figure 16: Determination of the gain variation coefficient in ADC unit as a function of the V_{op}. The ordinate axis on the right of the plot reports the estimated pixel gain as a function of Vi using the HG linearity results (see section 4.3.1).

The slope of the line, obtained interpolating linearly the points of Figure 16, gives the required $\frac{dG_{ADC}}{dV_i}$ coefficient:

$$\frac{dG_{ADC}}{dV_i} = 15.46 \ \frac{ADC}{V} \qquad (18)$$

From the above results the estimated gain variation for 100 mV variation of V_i is in average about 8%.

Gain adjustment "within channel" and "between channels" has been verified using four channels of the CITIROC evaluation board connected to four SiPM pixels and making use of the corresponding DAC-input measured linarites.

A description of the verification tests of the "within channel" and "between channels" gain adjustment is given in Annex C.

4.3.6 dG_{ADC}/dT Determination

The $\frac{dG_{ADC}}{dT}$ is determined using PHDs as produced by pulsing a blue LED at a constant rate of 10 kHz and time-on duration of 11.5 ns. The V_i is kept at 74.31 V and the temperature is increased with step of about 1 °C from 13 °C to 17 °C with accuracy of ± 0.1 °C. The DAC input is set to 126. One of the four available SiPM logical pixel is connected to channel 22 of the CITIROC evaluation board. The resulting PHDs are shown in Figure 17.

Using (7), the plot of the mean distances between subsequent local maxima and associated standard deviation errors for each of the histograms of Figure 17 is shown in Figure 18.

The slope of the line, obtained interpolating the points of Figure 18, gives the required $\frac{dG_{ADC}}{dT}$ coefficient:

$$\frac{dG_{ADC}}{dT} = -1.06\ \frac{ADC}{°C} \qquad (19)$$

A simple calculation using (8) and (9) gives the temperature coefficient, i.e. the variations of the V_i with T:

$$\left(\frac{dG_{ADC}}{dV_i}\right)^{-1} \cdot \frac{dG_{ADC}}{dT} = \frac{dV_i}{dT} = \frac{1}{15.46} \cdot -1.06 = -68.56 \pm 4.43\ mV/°C$$

The DAC-input values DAC_T corresponding to the k-th (k= 1,…..,64 PDM pixels) channel can be calculated as follows:

$$(a_k \cdot DAC_T + b_k) - (a_k \cdot DAC_k + b_k) = \frac{dV}{dT} \cdot \Delta T \quad (20)$$

where a_k and b_k are the slopes and intercepts of the DAC-input k-th channel, DAC_k the DAC code of the previously equalized k-th channel and $\Delta T = T_k - T_0$ are the differences between the k-th pixel temperature and the reference temperature respectively.

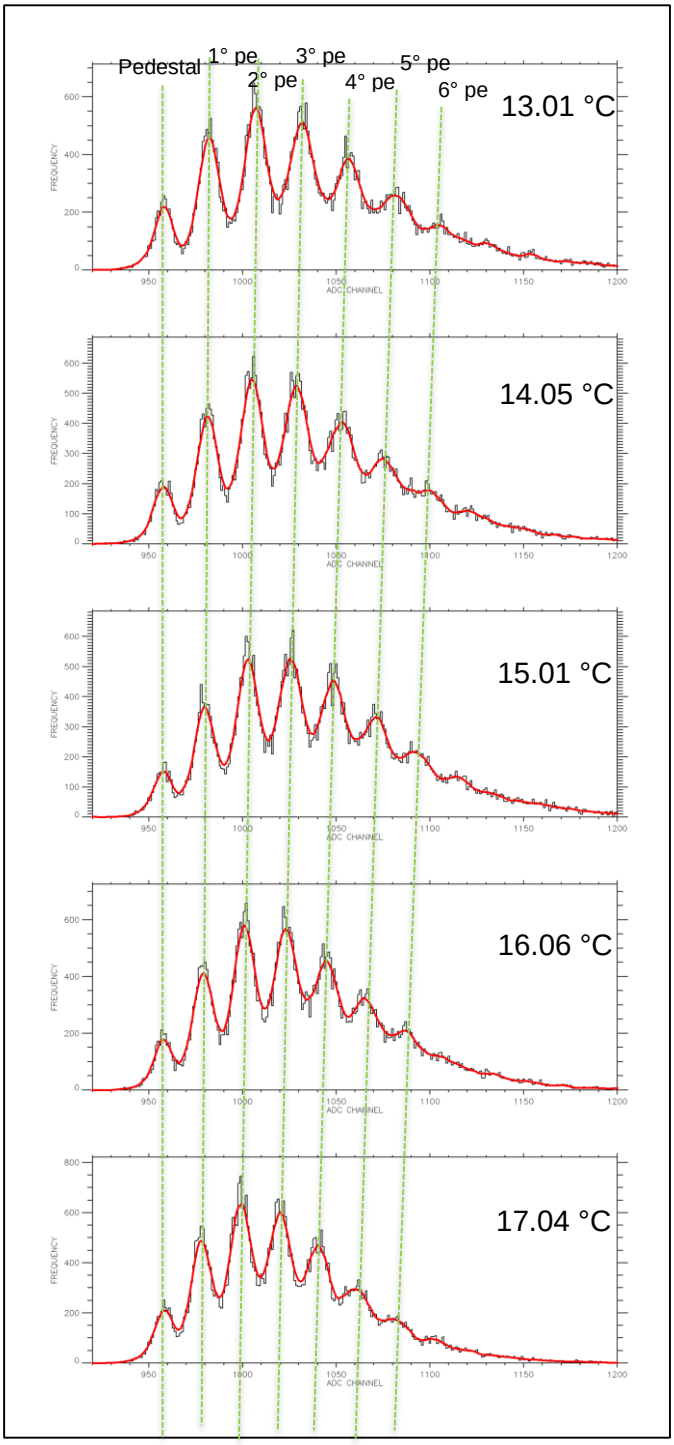


Figure 17: CITIROC Channel 22 PHD at a fixed V_i = 74.31 V as a function of the temperature. The increasing slopes of the hatching green lines show qualitatively the decreasing gain (distance between peaks), measured in ADC unit, as the SiPM temperature increases**.**

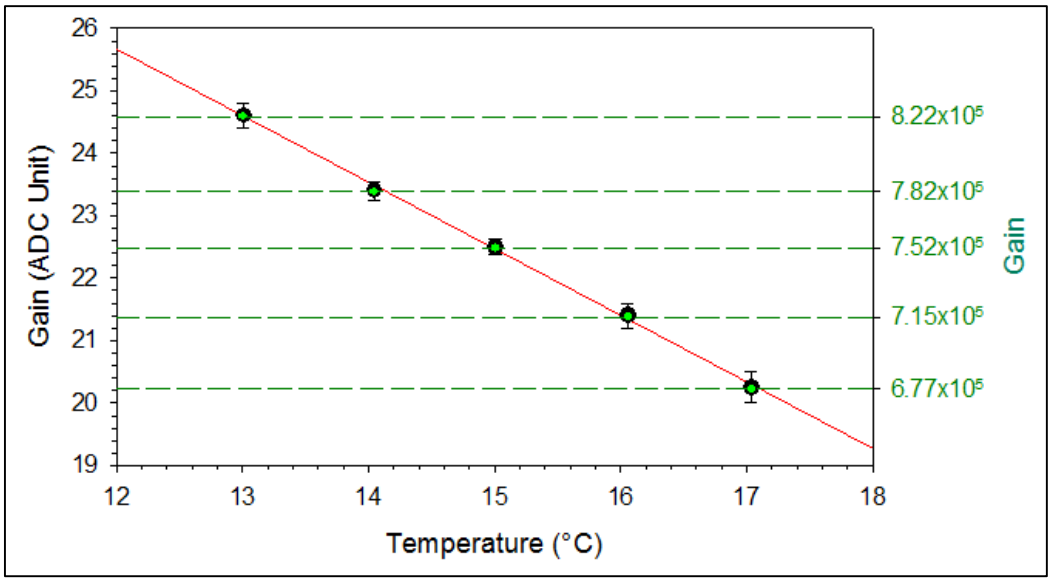


Figure 18: Determination of the gain variation coefficient in ADC unit as a function of temperature. The ordinate axis on the right of the plot reports the estimated pixel gain as a function of T_i using the HG linearity results (see section 4.3.1).

Resolving for DAC_T equation (20):

$$DAC_T = \frac{a_k \cdot DAC_k + \frac{dV}{dT} \cdot \Delta T}{a_k} \qquad (21)$$

Combining the temperature coefficient and the DAC-input linearity average slope, the temperature resolution for the system is of about 0.25 °C/DAC code.

A description of the “within channel” and “between channels” verification tests concerning gain adjustment as a function of temperature is given in Annex D.

4.3.7 Trigger signals equalization

As shown in Figure 2, digital trigger signals are generated when the analog input signals exceed a set threshold level in the discriminators. The ideal situation would be to have an equal response from all trigger channels for a given trigger threshold. In reality, small differences between channels due to the ASIC processing technology, produce a non-uniform response at the nominal threshold. CITIROC, however, is capable to compensate this trigger non-uniformity using for each channel a 4 bits–DAC with the aim to finely adjust and hence equalize the trigger response at the given threshold levels. It is worth to remember that any of 4 adjacent pixels, set to an equal threshold and for any PDMs, generates the first trigger level of the camera. This specific trigger

configuration mitigates, for some extent, the requirement for fine triggers equalization. However, since less stringent trigger setting could be used for others calibration needs, trigger signals equalization is simply performed. It must be said that the 4-bit DAC need to be set once and for all, thanks to the stability of the DAC with the temperature.

Trigger signals equalization is determined basically performing Fiber Stair measurement after doing gain equalization. The used method is the following:

Perform the Fiber Stair measurement with 4 bits-DAC=0 (pulsing LED at 500 kHz and increasing the threshold by one 10 bits-DAC per sampled point in a time window of 3 seconds). Repeat the Fiber Stair Increasing the 4 bits-DAC with steps of 4 DAC code until to DAC code 15. Figure 19 shows the four superimposed integral trigger rates for channel 11. Differentiating and inverting the trigger rate curves, as shown in Figure 20, the obtained histograms represent the distribution of the photons emitted by the LED pulses and then converted in pe by SiPM photocathode. The peaks of the smoothed histograms represent the number of pe detected.

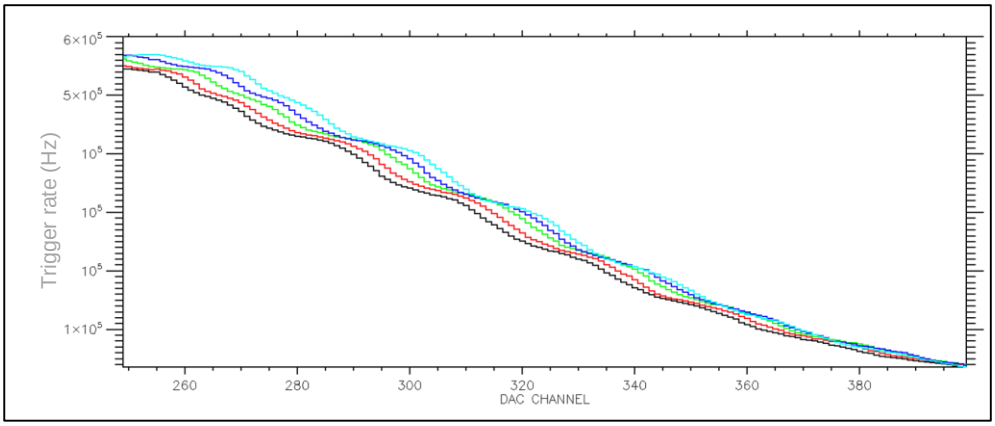


Figure 19: Channel 11 Fiber Stairs. Trigger rate as a function of 10 bits-DAC code for the 4 bits-DAC increments (0, 4, 7, 11, and 15).

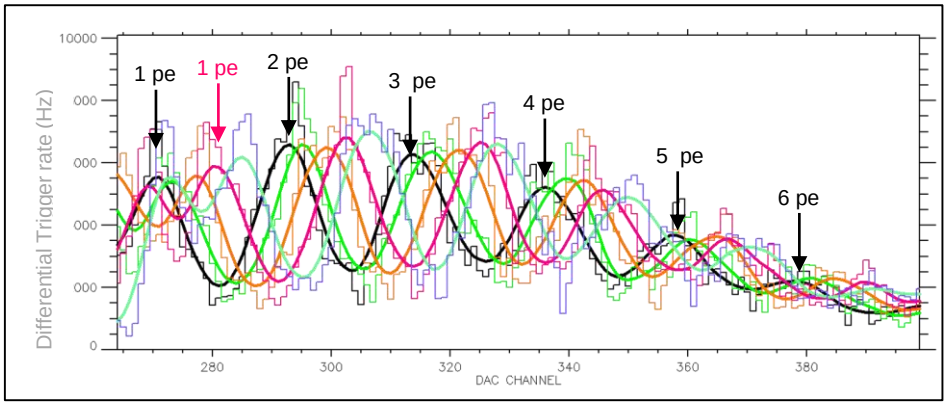


Figure 20 : Differential trigger rate varying the 4 bits-DAC in steps of 4 DAC code. An increasing in the 4 bits-DAC code turns out in a shift of the *pe* peaks in the abscissa.

By averaging the relative displacements on the abscissa of each corresponding pe peaks and plotting them as a function of the 4 bits-DAC steps we obtain:

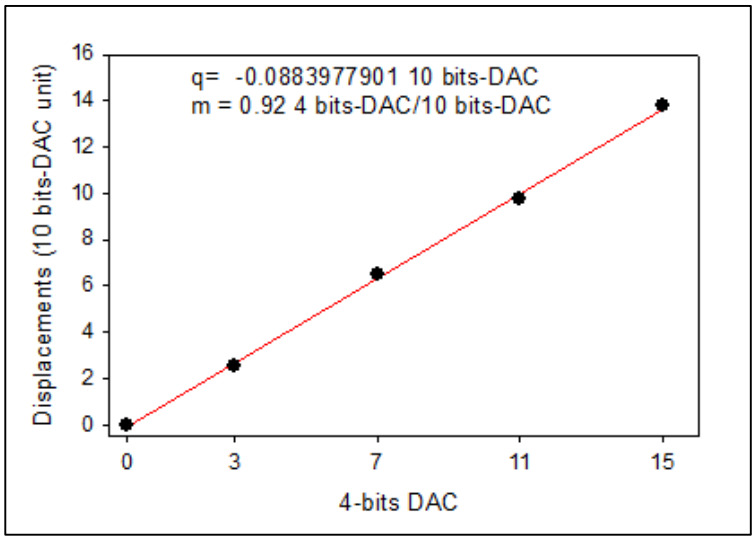


Figure 21: 4 bits- DAC linearity.

Fitting the data points to a line we obtain:

$$Disp\_DAC_{10\,bits} = m \cdot DAC_{4bits} + q \qquad (22)$$

Resolving the (22) for DAC_{4bits} we can equalize each trigger channel setting the corresponding 4 bits-DAC code according to the related trigger displacements as reported in Annex E.

5. CALIBRATION PROCEDURES

This section is devoted to a more practical/technical discussion on the procedures to be used for PDMs functional tests and contemporarily for performing relative calibrations. Figure 22 shows the work flow of the integration and verification activities for the ASTRI camera as defined in [RD8].

The accomplishment of the PDM tests is obviously directly correlated to the tests equipment. For a most effective and faster outcome the tests equipment and the set-up being used will be the ones already used for the tests performed with the CITIROC evaluation board.

The flow diagrams of Annex E are related to the set-up described in section 4.2 with minor modifications mainly concerning PDM cabling and pulse light generation. The operator(s) in charge of tests must pay attention to few but important things as temperature stability of the light-tight box, silica gel effectiveness (renew it when degraded) used to dry the box and instrumentation cabling. All the others parameters, as for example, pulse generation frequency and duration, SiPM operating voltages and temperature sensor calibration curves are codified and/or deduced by "ad hoc" application software.

Temperature calibration tests are also required because only one temperature sensor per PDM (the central one) is calibrated. A flow diagram of the temperature sensors calibration is described in Annex E.

A list of the software used for the PDM tests can be found in Annex G.

It is also of fundamental importance, for the part concerning the relative calibration, that the measurements of the DAC-input Voltages as function of DAC code are performed carefully. The ability to equalize pixels gains and compensate gains at different temperatures depends on the accuracy of how DAC-input curves are measured, so is important to pay attention at these measures.

The PDMs tests are the basis of further tests. The camera system test and the camera integration will be easier to surpass if PDMs are before tested. Test criteria are defined in order to guide in the selection of predefined fixed choices. No more than one channel (pixel) per PDM (64 channels) should be faulty, whatever is the cause of fault. Obviously faulty channels must be, after identification, saved to the “channel fault report file” to be used at data analysis time.

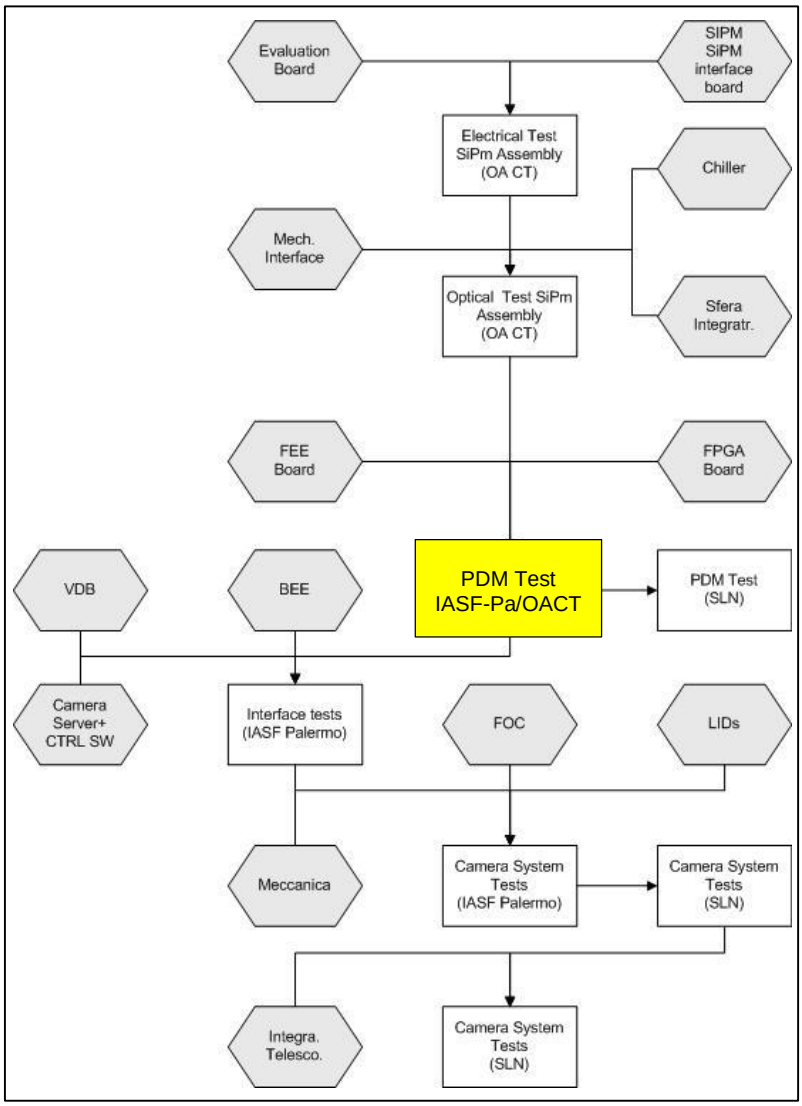


Figure 22: Sequence of activities to be performed for camera integration and verification. The highlight yellow box concerns the PDM test.

6. RELATED QUANTITIES & ERROR BUDGET

A direct consequence of measurements are quantities which, in the proper units, are used to describe their measure. Many of these quantities are related to each other, and as a result, relationships between them can be expressed by means of suitable equations. Intrinsically any measurement is affected by systematic errors (accuracy), namely bias i.e. the proximity of measurement results to the true value. It is useful to quantify the expected accuracy on the measured quantities involved in the measurements with the so called “Error Budget” table.

6.1 Related Quantities

Table 3 gives the measured quantities that can be related to each other.

Table 2

QUANTITY	MEASURED	UNIT
$\frac{dG_{ADC}}{dV_i}$	15.46	$\frac{\mathrm{ADC}}{\mathrm{V}}$
$\frac{dG}{dV_i}$	$51.68\ 10^4$	$\frac{k}{\mathrm{V}}$
$\frac{dG_{ADC}}{dT}$	-1.06	$\frac{ADC}{°C}$
$\frac{dG}{dT}$	$3.62\ 10^4$	$\frac{k}{°\mathrm{C}}$
$\frac{dV_i}{dT}$	-68.56 ± 4.43	$mV/°C$
$\frac{dV_{DAC\_input}}{dDAC\_input}$	0.016	V/DAC

6.2 Error Budget

The error budget provides an estimate of potential errors within the end to end electronics chain including SiPM that lead to deviations from the "true" energy determination ($\propto$ to the number of photo-electrons). Table 3 gives an estimation of the major error sources and the resulting accuracy.

Table 3

Error Source	Value	Accuracy (%)
SiPM power supply ripple	± 10 mV	± 0.8
Pulse Height ADC	12 bits ± ½ bit	± 0.5
Temperature sensors	± 0.2 °C	± 1.1
DAC-input gain adjustment	8 bits ± 1 bit	± 1.3
SiPM $<V_{op}>$ within pixel	see sect. 4.1	± 2.0
TOTAL		± 2.7

Another source of systematic error is the excess noise factor of the SiPM. For some extent, this can be statistically corrected measuring the cross talk probability at a given V_{op}.

ANNEX A

As described in section 4.1 all the pixels operating voltage are in the range of 71 V < V_{op} < 73.5 V when measured at 25°C and gain of 7.5 x10^5. Keeping the gain at 7.5 x10^5 and setting the temperature at 15 °C the resulting V_{op} lies between 70.2 V and 72.7 V as shown in the histogram of Figure A1. Details of how this operation is performed are given in sections 4.3.4, 4.3.5 and 4.3.6.

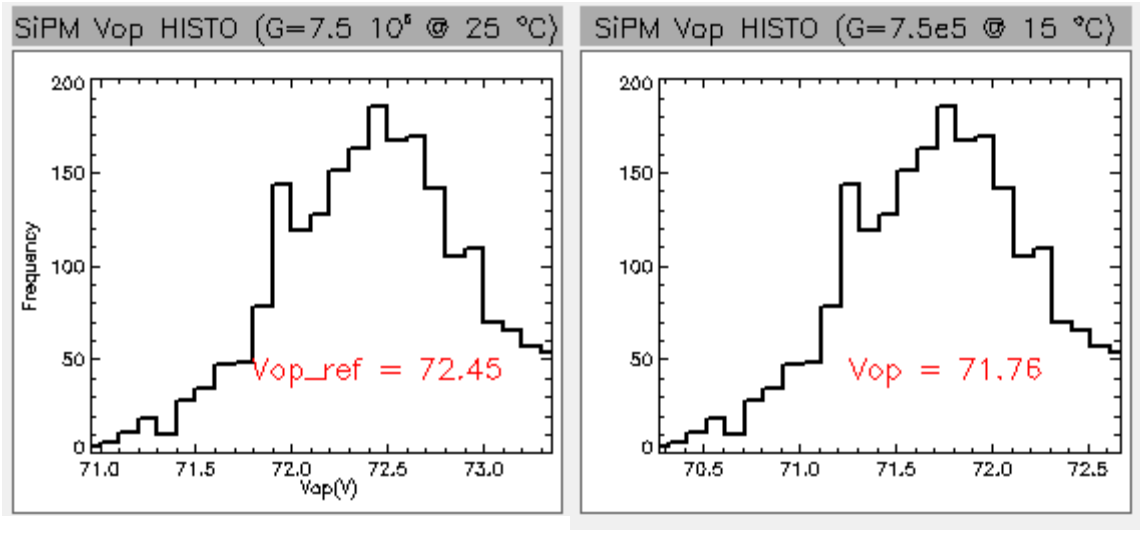


Figure A 1: Histograms of all pixel V_{op} at 25 °C and 15 °C. The histogram on the right of the figure has been obtained applying the equations (16) and (21).

ANNEX B

CROSS-TALK PROBABILITY EVALUATION

When light enters one SiPM micro-pixel, there may be cases where a pulse of 2 pe or higher is produced. This happens because secondary photons are generated in the avalanche multiplication process of the SiPM micro-pixel and those photons are detected by other micro-pixels. This phenomenon is called “optical cross-talk”. The cross-talk probability has almost no dependence on the temperature within the rated operating temperature range. The probability that the cross-talk occurs increases as the V_{op} is increased.

Among different definitions of the optical crosstalk, we define the crosstalk probability as:

$$P_{cross-talk} = \frac{N_{\geq 2pe}}{N_{\geq 1pe}}$$

The usual way to evaluate the cross-talk probability is based on Stair measurement, i.e. measure the pulses rate as function of threshold (10 bits-DAC) in dark ambient. A Stair measurement of the pixel connectet to channel 22 of CITIROC is shown in Figure B1 with V_i = 74.31 V.

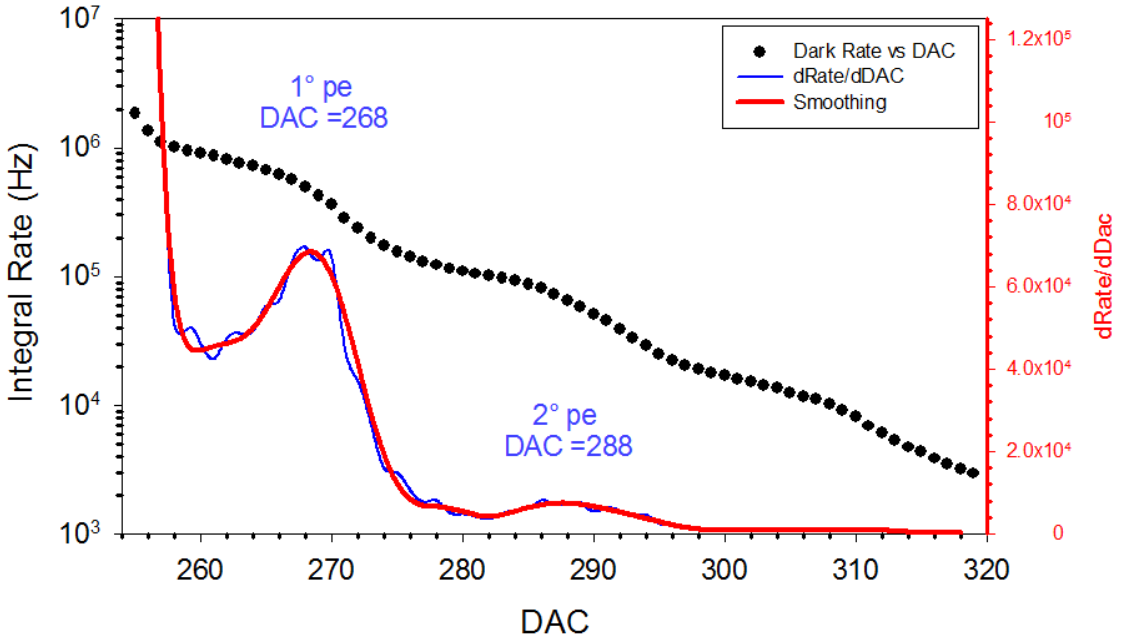


Figure B 1: Stair measurement and differentiated rate vs DAC.The relative maxima are found at DAC=268 and DAC=288 for the 1st and 2nd pe respectively.

Differentiating the integral rate and changing the sign, the relative maxima of the obtained smoothed curve correspond to the 1st and 2nd pe. The DAC codes for the 1st pe and 2nd pe are now used to evaluate the cross-talk probability as follows:

a) Divide the integral rate values for the rate value corresponding to the DAC code of the 1st pe multiplying them by 100 and posing to 100 all the resulting values greater than 100.
b) Find on the normalized integral rate curve the value corresponding to the DAC code of the 2nd pe. This represents the cross-talk probability.

Figure B2 shows graphically the used method and the cross-talk probability that results to be about 13%.

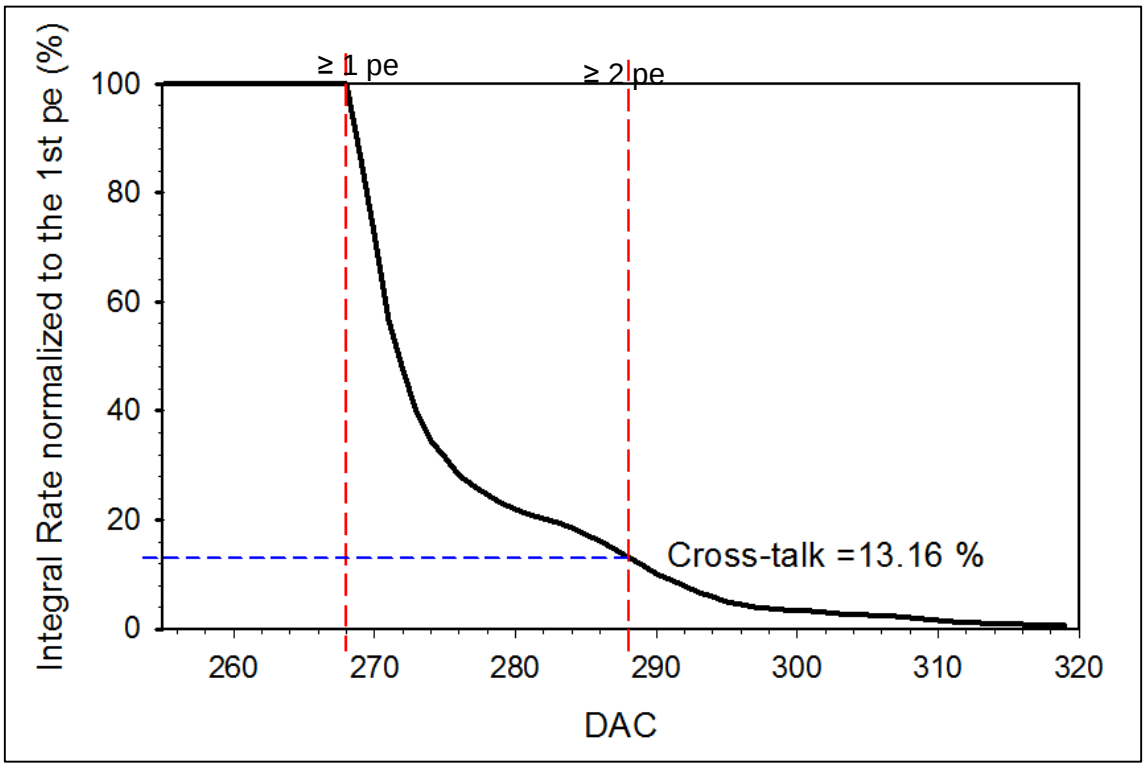


Figure B 2: Graphical representation of the method used for cross-talk evaluation.

ANNEX C

WHITHIN CHANNEL

PHDs of channel 22 at V_{i0} =74.31 V and V_{i0}=74.51 V with DAC-input = 126 for both are shown in Figure C1. As it is evident from the Figure C1 and recalling that the distances between peaks are proportional to the SiPM gain, a change in V_{i0} produces a change in the gain.

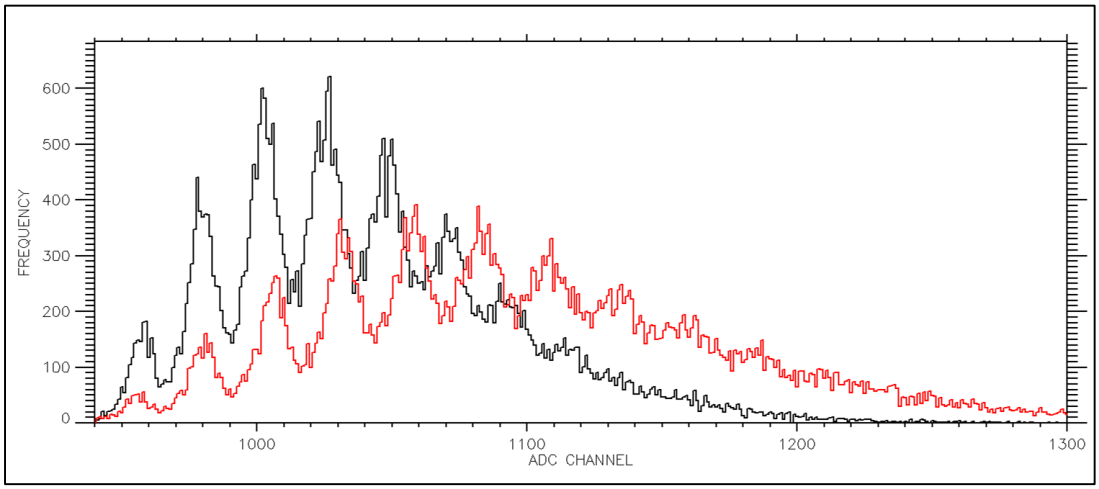


Figure C 1: PHDs for the same channel (pixel) with V_{oi}= 74.31 V (black histogram) and Voi =74.51 V (red histogram). DAC-input value=126 for both PHDs.

Applying the (16) and being $V_{op0} = V_{opk}$, $b_0 = b_k$, $a_0=a_k$ and DAC_0 =126 the resulting integer DAC_k value is:

$$\mathrm{DAC_k} = \frac{(74.51 - 74.31) \; - \; 0.0156 \cdot 126}{- \, 0.0156} = 114$$

The DAC-input value for channel 22 can be then modified according to this result. We expect that the PHD with V_{i0}=74.51 V and DAC-input value = 114 will be, within a ± ADC/2 channel error, the same of the PHD with V_{i0}=74.31 V and DAC-input value = 126.

Figure C2 shows the PHDs related to the above setting.

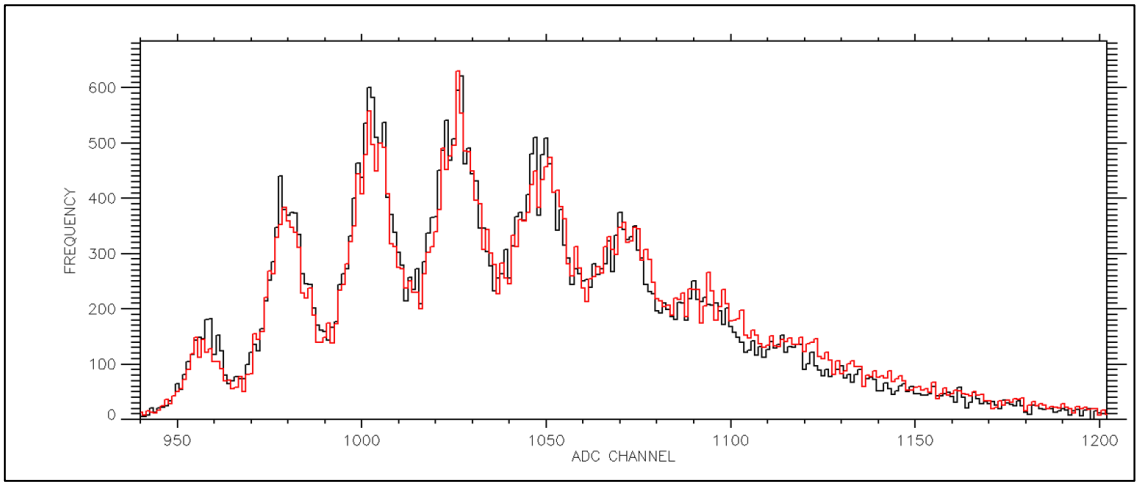


Figure C 2: PHDs for the same channel (pixel) with V_{oi}=74.31 V (black) and V_{oi}=74.51 V (red). DAC-input value=126 and 114 respectively.

The average distances between peaks, see (17), are 23 and 22.8 ADC units respectively, well inside the ± ADC/2 channel resolution.

BETWEEN CHANNELS

This verification test is applied to different channels (pixels) keeping the channel 22 as the reference channel. In this case for calculating the DAC_k, it is necessary to know the V_{opi} of each pixel and apply the (16) with $V_{i0} = V_{ik}$ and b_0, b_k, a_0 and a_k given by the respective DAC-input line fit related to the channel 21, 22, 23, 24. The applied V_{op} to the pixels connected to the channel 21, 22, 23 and 24 are: 71.78 V, 71.79 V, 71.77 V and 71.79 V respectively, with $V_{i0}=V_{ik}$=74.31 V. The PHDs of the four channels (pixels) are shown in Figure C3. Note the different pedestal position for each channel due to different bias voltage of the CITIROC channels.

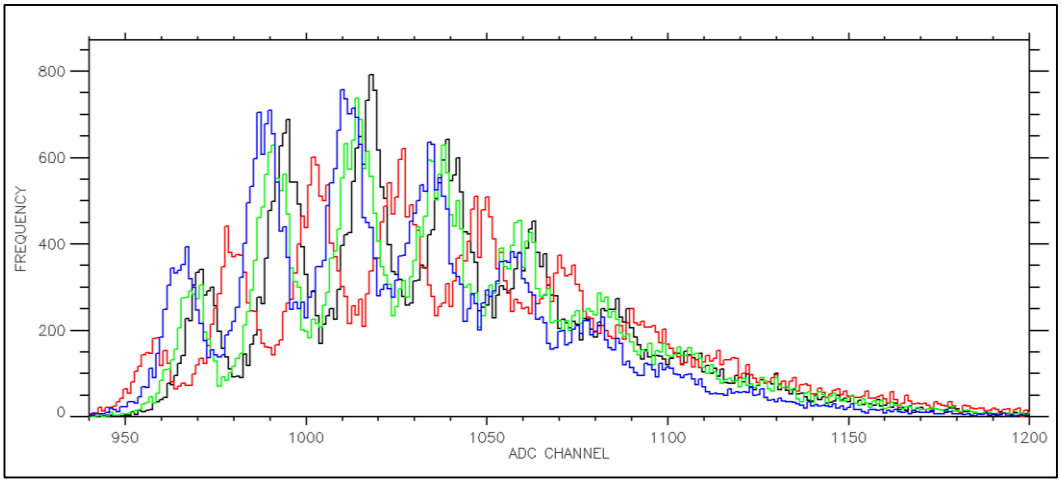


Figure C 3: Histograms of 4 pixels with different V_{op}..

Figure C4 shows the PHDs after correction of the gain by means of DAC-input of value of 120,126,123,116 respectively for CH 21, 22, 23, 24.

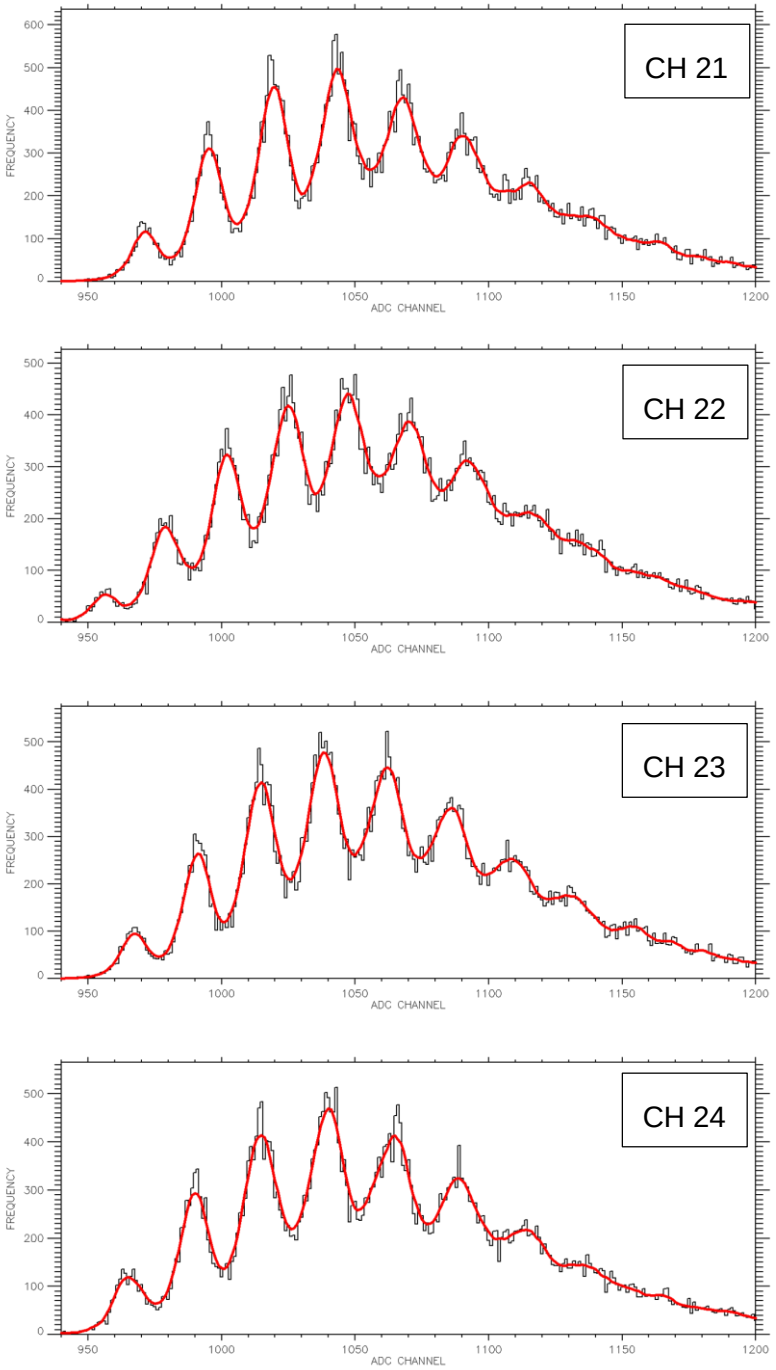


Figure C 4: Equalized gain “between channels” using DAC-input corrections.

Figure C5 shows PHD histograms with pedestals shifted with respect to the pedestal of channel 21 validating the gain DAC-input adjustment approach. The different height of the frequencies are due to the slightly not uniform illumination of the pixels by the LED.

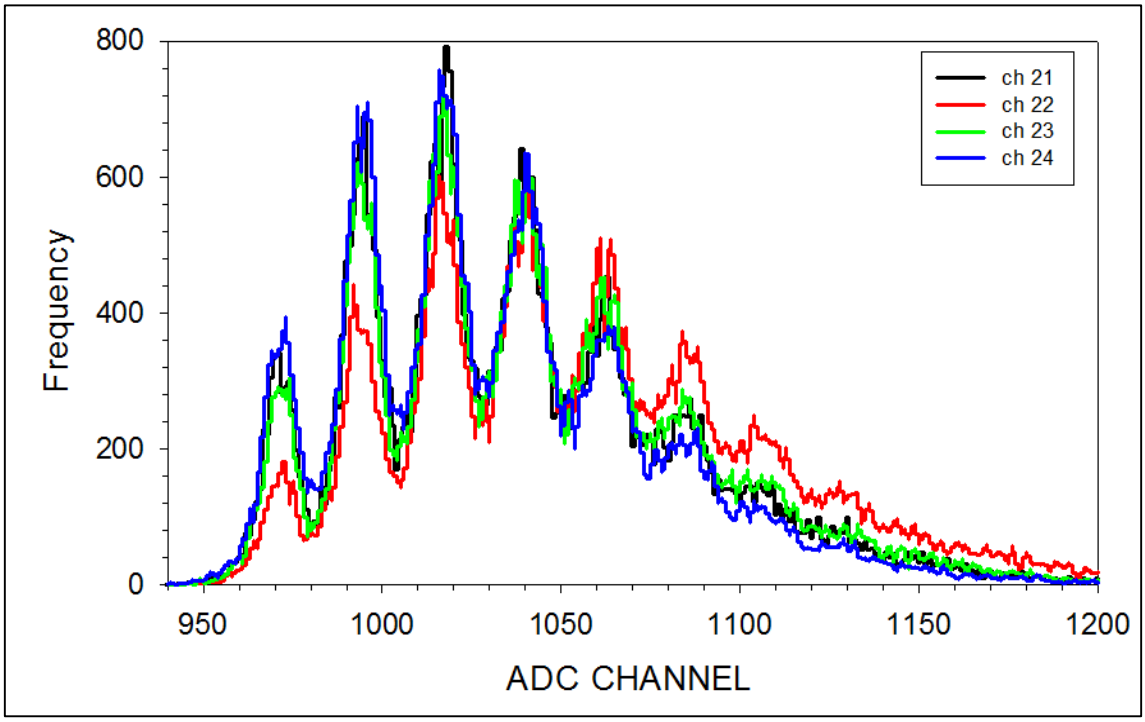


Figure C 5: Plot of the PHDs overlapping histograms shows a perfect “between channels” gain adjustments.

ANNEX D

WHITHIN CHANNEL

PHDs of channel 22 at V_{i0} =74.31 V, DAC-input = 126 and temperature T=15.01 °C and T= 17.04 °C are shown in Figure D1.

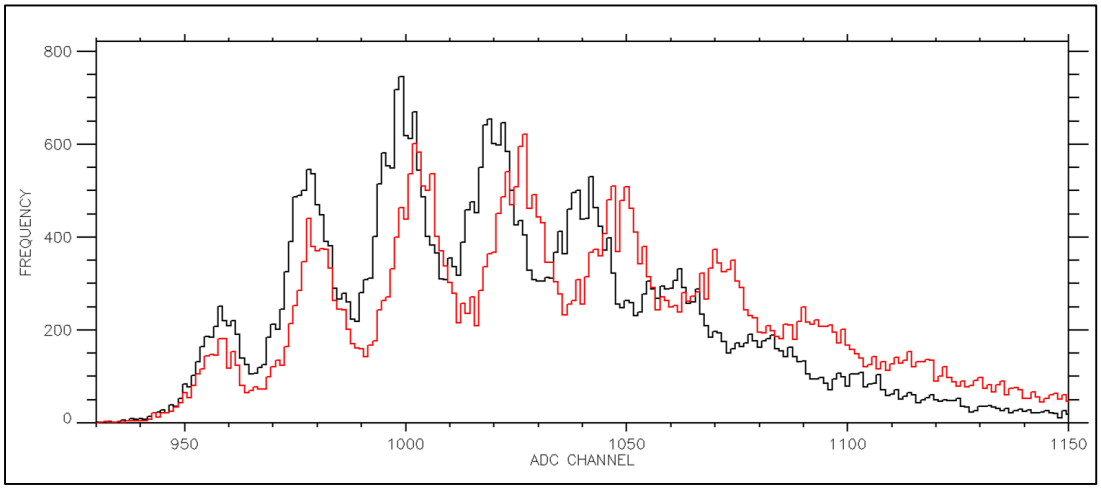


Figure D 1: PHD at T=15.01 °C (red histogram) and T=17.04 °C (black histogram) respectively.

As expected, the PHD at 15.01 °C shows a higher gain (distances between peaks) with respect to the one at 17.04 °C.

Applying the (21) and posing $a_0=a_k$ and $b_0=b_k$ (because we are using the same channel), the DAC_k results:

$$DAC_k = \frac{-0.0156 \cdot 126 - 2 \cdot 0.06856}{-0.0156} = 135$$

Setting the DAC_k value to 135, the PHDs became as shown in Figure D2:

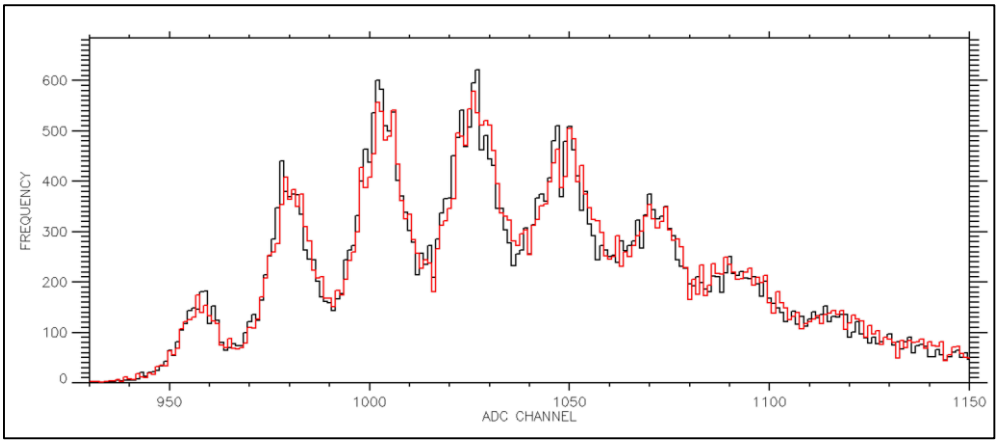


Figure D 2: PHD at T=15.01 °C (red histogram) and T=17.04 °C (black histogram) corrected for temperature.

BETWEEN CHANNELS

This verification test is applied to different channels (pixels) keeping the channel 21, 22, 23 and 24 at temperatures of 16.06 °C, 15.01°C, 14.05 °C and 13.01 °C respectively. The channel for reference gain remains channel 22 and the V_{i0} = 74.31 V for all the channels. The DAC_T value for each channel has been calculated applying the (21) and then set in the respective CITIROC DAC-input channels. Figure D3 shows the PHDs of the four channels (normalized to the ADC of the channel 22 pedestal) as obtained after data acquisition.

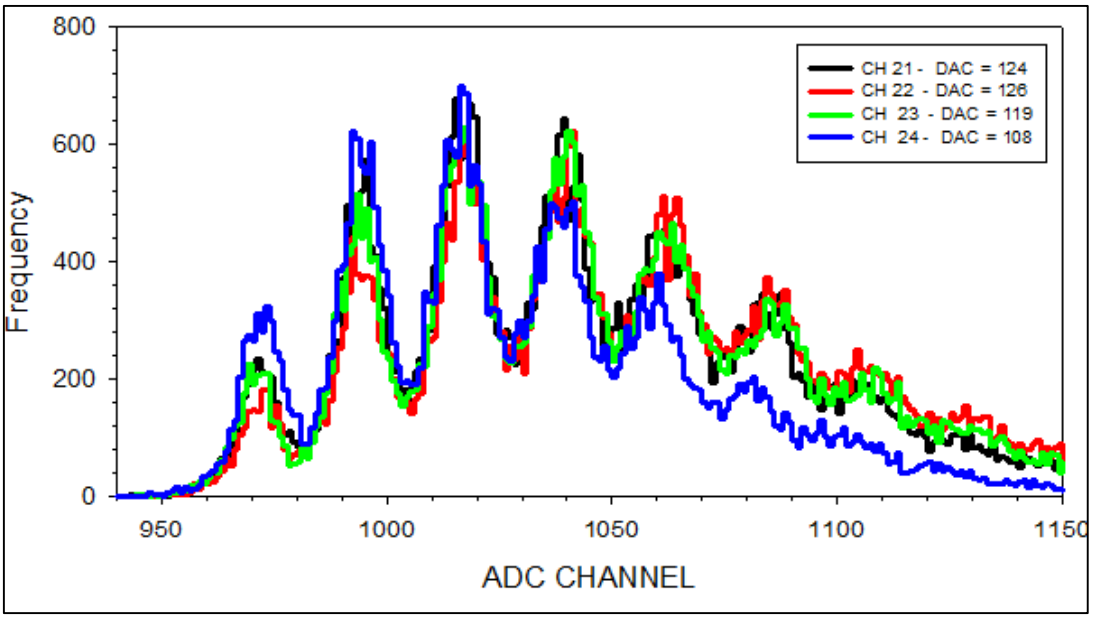


Figure D 3: Channel 21, 22, 23 and 24 PHDs corrected for temperature.

ANNEX E

Figure E1 shows the differences of the 10 bits-DAC for the CITIROC channels, 10,11,12,13. The maximum difference between channels is of about 6 DACs.

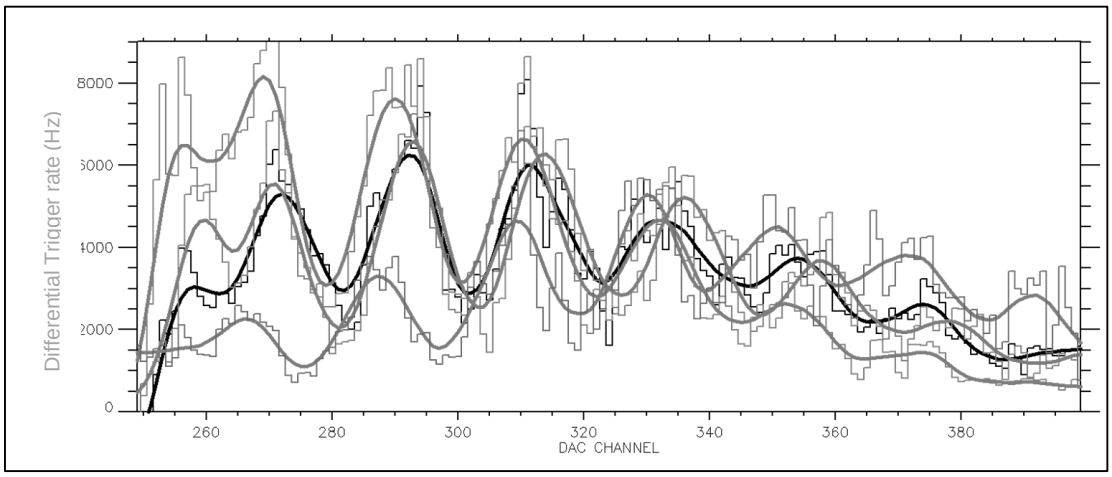


Figure E 1: Measurement of the trigger dispersion of 4 CITROC channels.

For equalizing the trigger signals we make use of the equation (22).

Equation (22) can be written as:

$$\mathrm{DAC}_{4\mathrm{bits}} = \frac{\mathrm{Disp\_DAC}_{10\ \mathrm{bits}} - \mathrm{q}}{m}$$

Substituting at m, q the numerical values found in section 4.3.7 and calculating from Figure E1 the relative $\mathrm{Disp\_DAC}_{10\ \mathrm{bits}}$ with respect to channel 11, the DAC code for the channel 10, 12, 13 are 5, 2, 1 4bits-DAC code respectively. Setting the 4 bits-DAC with the code found and rerun the Fiber Peq measurements we obtain the plot shown in Figure E2. As is clearly evident the 4 trigger channels are now aligned. This important result means that when a trigger threshold is set for all the 1984 pixels to a given value the dispersion around this value is given by the resolution of the 10 bits-DAC.

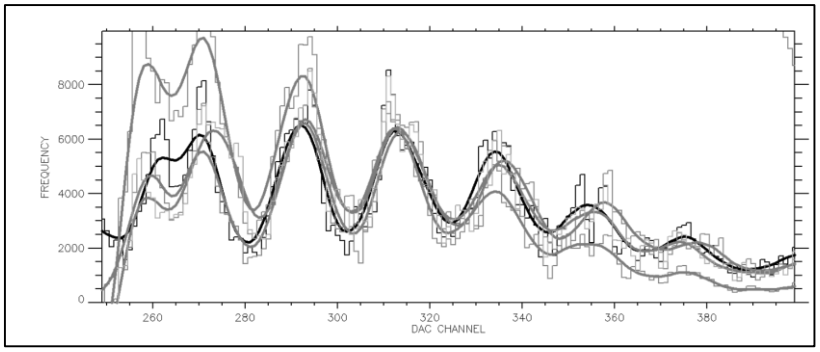
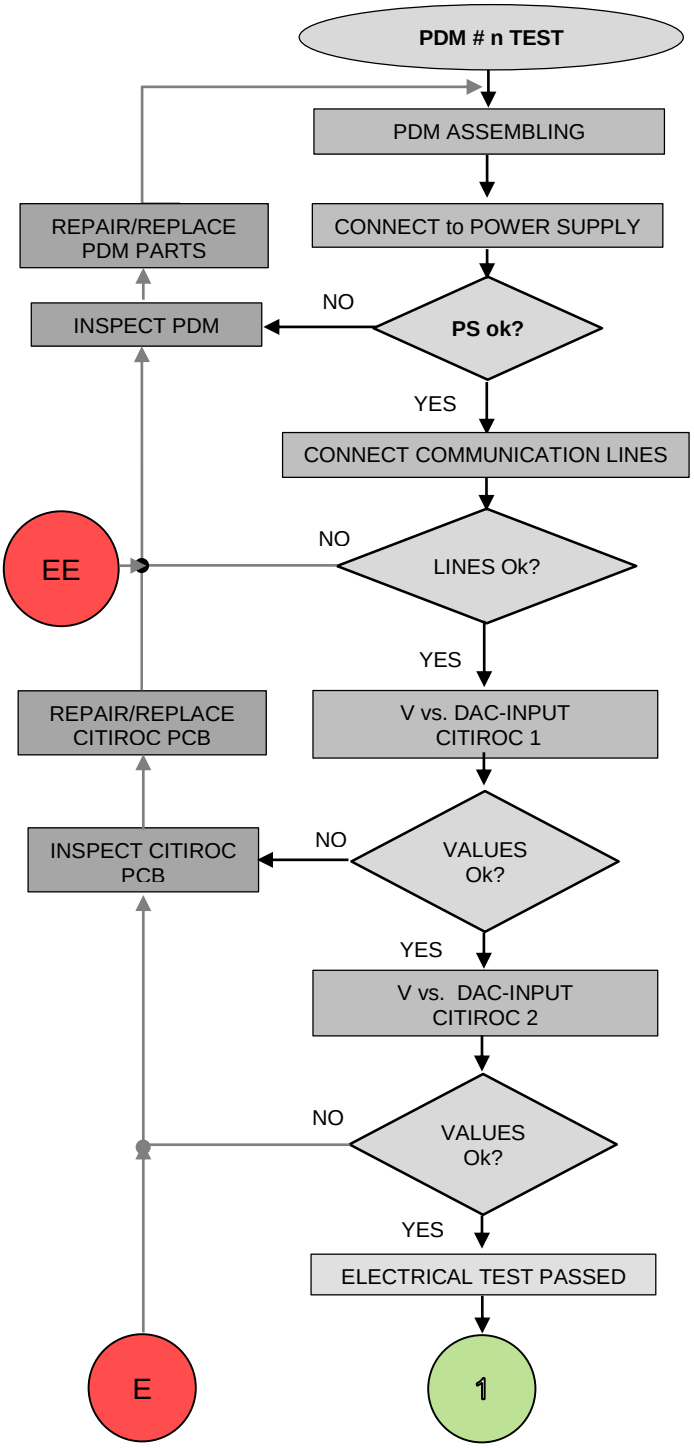


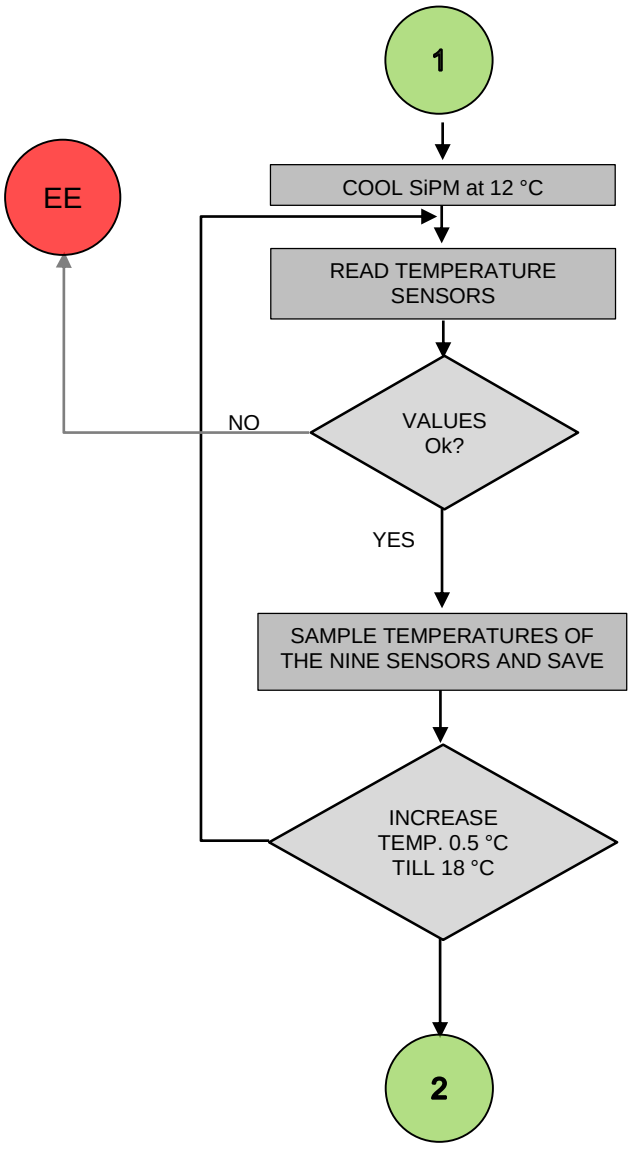
Figure E 2: Trigger equalization of four CITIROC channels.

ANNEX F

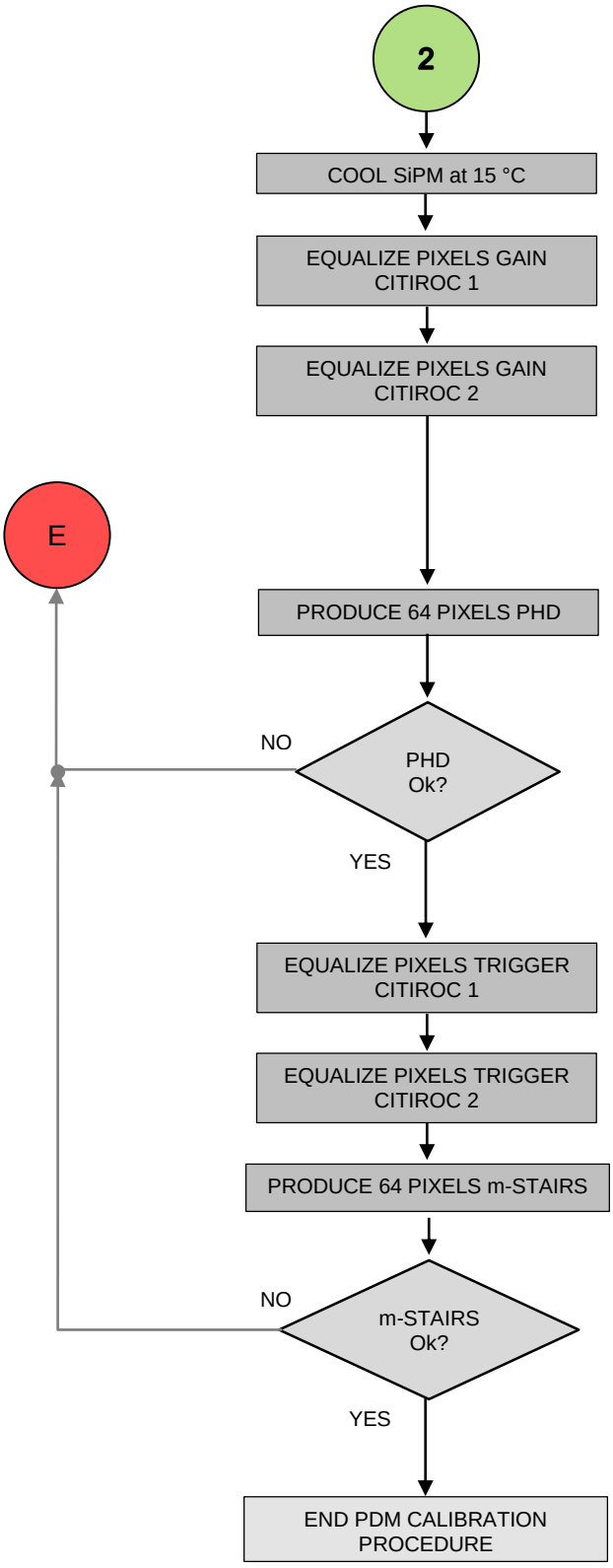
These flow diagrams show the needed steps to perform PDM functional tests as well as temperature sensor calibration and pixels gain and trigger equalization.



PDM ELECTRICAL TEST
Assembling mechanically the 3 PCBs forming the PDM and cabling them. Put PDM into opened light-tight box.
Connect the PDM to a power supply provided of current limiting capability and check that current absorption do not exceeds the typical operating currents (CITIROCs PCB =…..A, ATIX 7 PCB=…..A). SiPM voltage must be increased with a ramp function. If anomalous current(s) value(s) is (are) detected switch off power and start inspection and if necessary repair/replace module(s).
Connect serial communication cables and test if connections are active. In case of fault connection switch off power and start inspection and if necessary repair/replace module(s).
Start measurements of the DAC-input of CITIROC 1. If measured data are not compliant with the expected values switch off power and start inspection and if necessary repair/replace module(s).
Start measurements of the DAC-input of CITIROC 2. If measured data are not compliant with the expected values switch off power and start inspection and if necessary repair/replace module(s).
Save data to file DI_PDM_*nr1*_nr*2:* ***nr1=PDM_number*** ***nr2= CITIROC number in the PDM***
PDM electrical test passed.



PDM TEMP. SENSORS CAL.
Check Silica gel conditions. Renew it if necessary. Close light-tight box and cool SiPM at 12°C.
Run Temp_sensor program on PC. Read ADC values from temperature sensors. Check the consistency of the data. If data are non-consistent with the expected values something is wrong with SiPM board and/or ARTIX 7 and/or connections.
If data values are consistent then save the sampling ADC values in a file named: **PDM_temp_nr1:** **nr1=PDM_number**
Increase the temperature of SiPM increasing suitably the temperature of the light-tight box. Use step of 0.5 °C approximately up to 18 °C.
Save the file produced for further analysis and data fitting.
Pass to the next test



PDM RELATIVE CALIBRATION

Check Silica gel conditions. Renew it if necessary. Close light-tight box and cool SiPM at 15°C.

Run DACINPUT program on PC. Read provided PDM Vop file and set the new Vop, taking into account the desired temperature (15 °C is the baseline), setting DAC-input values in the slow control register. File with the DAC-input related to the CITIROC 1 and CITIROC 2 will be produced and saved with appropriate name:

PDM_*nr1*_nr*2:*
nr1=PDM_number
nr2= CITIROC number in the PDM

Start PHD run.

Check data values consistency.

If data values are not consistent with expected values something is wrong with CITIROC and/or ARTIX 7 and/or SiPM.

Set 4bits-DACs of CITIROC 1 to values calculated by 32 channel m-STAIRs curve.

Set 4bits-DACs of CITIROC 2 to values calculated by 32 channel m-STAIRs curve.

Produce PDM (64 pixels) m-STAIRS.

Check triggers alignment.

If data values are not consistent with expected values something is wrong with CITIROC and/or ARTIX 7 and/or SiPM else save data to file named:

PDM_trigger_nr1_nr2:

nr1=PDM_number
nr2= CITIROC number in the PDM

PDM calibration procedure ended.
TEST PASSED

ANNEX G

A couple of programs, designed to carry out operations for each specific application, assists the Lab. measurements. The programs, written in IDL, are:

DACINPUT.prj

FIT_MULTIPLE_GAUSSIAN.prj

A brief description is given below.

DACINPUT.prj

This application has to be used for PDM calibration as allows to determine the DAC-input code to be set for each channel (pixels) using the SiPM Vop files, DAC-input linearity files and a given operative temperature.

FIT_MULTIPLE_GAUSSIAN.prj

This application is a general purpose fitting program. It is useful to promptly fit and visualize the results from structured data as Dark PEQ, Fiber PEQ, Dark Stair and Fiber Stair.